ATARI™ — Kurz·Kasch, Inc.

COMPUTER GAMES OPERATORS HANDBOOK

INTRODUCTION

The age of video electronic amusement devices places unusual demands upon the service personnel who are connected with the industry. The electromechanical service personnel are now finding service problems steeped in complex electronic technology including digital logic. It is Atari's hope that this small booklet produced in cooperation with Kurz-Kasch Electronics will help simplify the day-to-day maintenance problems you face in the field. This booklet is in no way intended to be a complete course in digital logic or television diagnostics. It is hoped, however, that the material presented here will help you overcome the trials of maintenance within this new era of video/computer technology.

Kurz-Kasch Electronics is dedicated to producing efficient and versatile digital test equipment and making it available to designers and field engineers at a price which represents a realistic combination of quality and required accuracy.

The logic probes are instruments which give answers. No interpretation or interpolation is required when testing or trouble-shooting digital circuits.

Through the Electronics Division's Center for Technical Development, home study courses are offered to keep engineers and field service personnel abreast of the changing technology. The courses are also designed to transition one from electronic, electrical and/or electromechanical skills to the digital logic domain.

Our engineers are working on tomorrow's test equipment and training material today.

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LOCATION TABLE

The following chart is intended to give the operator a method for evaluating his chosen location as to the relative earning capacity of our games and a relative longevity of same applied to his location. The top number indicates an initial earning capacity and the bottom number indicates the expected longevity. This is only a relative measure.

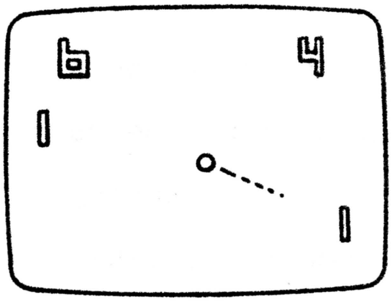
	Neighborhood Lounges	Young People's Bars	Arcades	Amusement Parks	Bowling Alleys	Skating Rinks	Retail Stores	Hotel Lobbies	Gas Stations
PONG	6 / 2	7 / 5	6 / 6	7 / 6	6 / 3	6 / 3	5 / 4	5 / 5	3 / 3
PONG DOUBLES	7 / 4	7 / 6	6 / 6	7 / 6	7 / 4	6 / 3	4 / 4	6 / 5	3 / 3
SUPERPONG	6 / 2	8 / 6	6 / 6	7 / 6	6 / 3	6 / 3	5 / 4	5 / 5	3 / 3
QUADRAPONG	6 / 4	*7 / 5	5 / 5	5 / 5	5 / 3	5 / 3	2 / 1	6 / 4	2 / 1
SPACE RACE	4 / 1	4 / 2	6 / 5	6 / 6	6 / 3	6 / 2	5 / 5	3 / 1	2 / 2
GOTCHA	3 / 1	6 / 4	5 / 4	6 / 3	5 / 3	5 / 3	4 / 2	5 / 2	3 / 3
COLOR COTCHA	3 / 1	6 / 4	6 / 5	7 / 3	5 / 3	5 / 3	4 / 2	5 / 2	3 / 3
WORLD CUP	6 / 5	7 / 5	5 / 5	5 / 5	5 / 3	5 / 3	2 / 1	6 / 4	2 / 1
REBOUND	5 / 4	7 / 7	5 / 3	5 / 3	5 / 3	5 / 3	4 / 2	8 / 5	4 / 1
GRAN TRAK 10	6 / 5	10 / 8	10 / 8	9 / 8	9 / 8	9 / 8	6 / 5	7 / 6	6 / 5

*Income at 25¢ for four (4) players better.

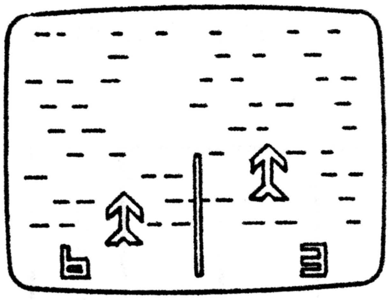
The above ratings are relative to a scale where one (1) is low and ten (10) is high.

EXHIBIT 6

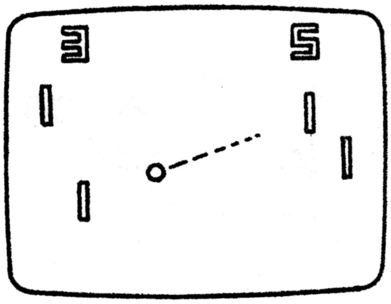
THE GAMES PEOPLE PLAY...



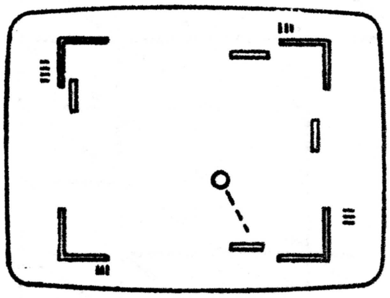
PONG -- The "grandfather" of all paddle games... Two players play a simulated game of ping-pong. Ball serves automatically out of the net, with realistic "pock" sounds when hit. Game is played to a single-player score of 11 or 15 (operator adjustable).



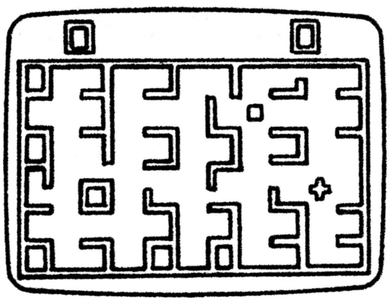
SPACE RACE -- Two player game with space ships racing across the galaxy, dodging meteors and asteroids. When ships connect with asteroids, they disintegrate and the ship is relocated at the bottom of the screen. One ship aims to reach the top of the screen before the other. Each ship attaining this scores a point.



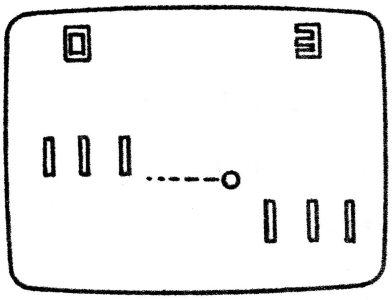
PONG DOUBLES -- This version of "Pong" enables two or four players to play a competitive tournament, with all the realism of a game of double ping-pong.



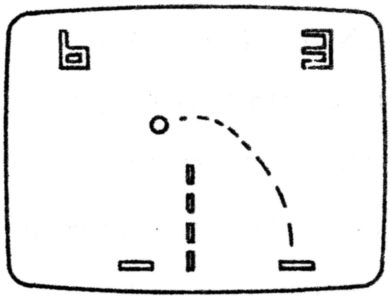
QUADRAPONG -- A two or four-player video game, with a video ball bouncing from side to side off the four walls of the screen trying to penetrate each player's goal. Bleeping sounds. Players start with four points each and lose one each time another player enters their goal, until eventually all players are eliminated except one -- the winner.



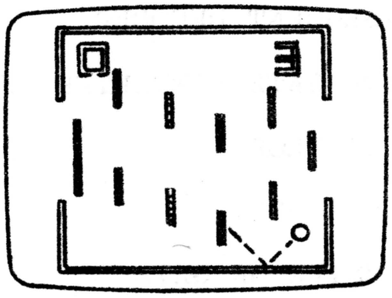
GOTCHA -- A two-player game where the "chaser" pursues the "chasee" represented by a square and a plus-sign. Maze is ever-changing, with electronic "bleep" when chasee is caught and chaser wins a point. Each time there is a catch, the point is scored, the screen wipes clean, and the chase begins all over again. Players then reverse roles and the game is on again.



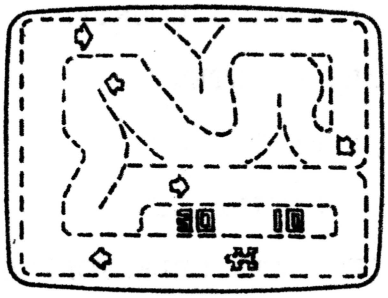
SUPERPONG -- In this game, two players try to coordinate three simultaneously-moving paddles each, keeping the ball going over the net. Ball is served from anywhere on the screen once a player misses a serve, adding to the unknown anticipation of excitement. Sound effects.



REBOUND -- A two-player game that simulates all of the action of a real game of volleyball. Net grows as volleys increase; player gets score when opponent misses the ball. Three hits on each side of net; fourth is a miss that scores for opponent. Putting "english" on the paddle determines vector.



WORLD CUP FOOTBALL -- The first video game that allowed the player to actually "catch" and kick-return the ball, aiming for the opponent's goal. Designed for one to four players with each player controlling two forwards, two defensemen, and one goalie. Electronic "bleeps" when caught or kicked. Accurately portrays a game of soccer.



GRAN TRAK 10 -- Video games enter the second generation with GT10 - the first computer game that simulates all the dynamics of Gran Prix racing...a steering wheel, 4-speed gear shift, accelerator pedal and brake all work to control the video-generated car. Electronically-created sound effects build excitement and realism.

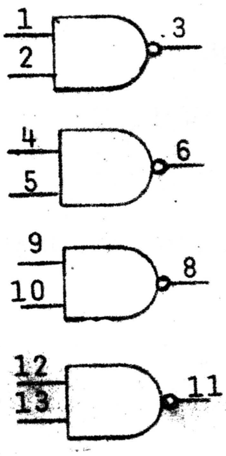
ATARI™

MORE.....The reservoir of game ideas is limited only by the imagination of people that play games. In excess of ten new game concepts are constantly in various stages of laboratory development at Atari, cycling through the intricate process of matching concept to psychological game parameters, realistic engineering, design and production prototyping.

7400	72000	QUAD 2-INPUT NAND GATE
7402	72001	QUAD 2-INPUT NOR GATE
7404	72002	HEX INVERTER
74S04	72049	HEX INVERTER
7408	72027	QUAD 2-INPUT AND GATE
7410	72003	TRIPLE 3-INPUT NAND GATE
7413	72050	DUAL NAND SCHMITT TRIGGER
7420	72004	DUAL 4-INPUT NAND GATE
7425	72005	DUAL 4-INPUT NOR WITH STROBE
7427	72006	TRIPLE 3-INPUT NOR GATE
7430	72007	SINGLE 8-INPUT NAND GATE
7448	72008	BCD TO 7-SEGMENT DECODER
7450	72009	DUAL AND/OR GATE (INVERTER/EXPANDER)
7474	72010	DUAL D FLIP FLOP
7483	72011	4-BIT FULL ADDER
7486	72012	QUAD EXCLUSIVE OR GATE
7490	72013	DECADE COUNTER
7492	72038	DIVIDE-BY-(2-6-12) COUNTER
7493	72014	4-BIT BINARY COUNTER
74107	72015	DUAL JK M/S FLIP FLOP
74153	72016	DUAL 4-BIT MULTIPLEXER
74157	72025	QUAD 2-INPUT DATA SELECTOR/MULTIPLEXER
74165	72033	PARALLET-LOAD 8-BIT SHIFT REGISTER
74192	72032	SYNCHRONOUS DECADE UP/DOWN COUNTER
74193	72035	SYNCHRONOUS BINARY UP/DOWN COUNTER
LM380	72048	AMPLIFER

NE555	72018	TIMER
NE566	72021	FUNCTION GENERATOR
747	72045	DUAL OPERATIONAL AMPLIFIER
RC4136D	72052	QUAD OPERATIONAL AMPLIFIER
MFC6040	72042	VOLTAGE CONTROLED OPERATIONAL AMPLIFIER
8098	72032	HYBRID
8103	72029	HYBRID
8099	72029	HYBRID
9311	72023	ONE-OF-SIXTEEN DECODER/DEMULTIPLEXER
9312	72024	8-INPUT MULTIPLEXER
9314	72036	QUAD LATCH
9316	72017	4-BIT BINARY COUNTER
9321	72031	DUAL ONE-OF-FOUR DECODER
9602	72026	DUAL MONOSTABLE MULTIVIBRATOR
74186	74186	ROM

7400
QUAD 2-INPUT NAND GATE



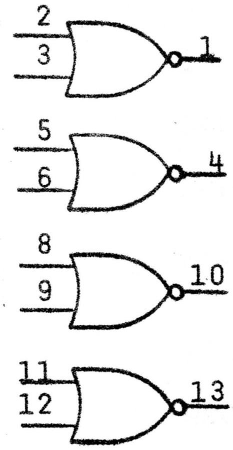
TRUTH TABLE

INPUTS		OUTPUT
1	2	3
0	0	1
0	1	1
1	0	1
1	1	0

VCC PIN 14

GND PIN 7

7402
QUAD 2-INPUT NOR GATE



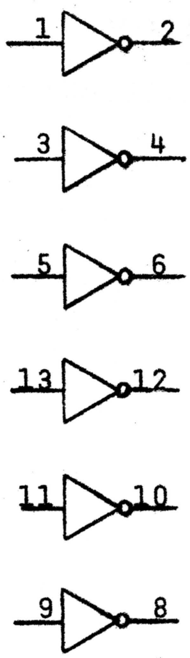
TRUTH TABLE

INPUTS		OUTPUT
2	3	1
0	0	1
0	1	0
1	0	0
1	1	0

VCC PIN 14

GND PIN 7

7404/74S04
HEX INVERTER



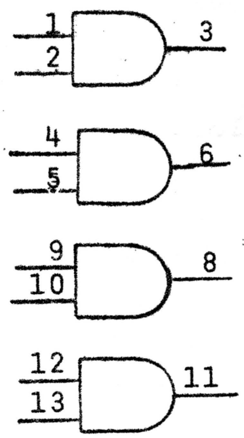
TRUTH TABLE

PIN	
1	2
0	1
1	0

VCC PIN 14

GND PIN 7

7408
QUAD 2-INPUT AND GATE



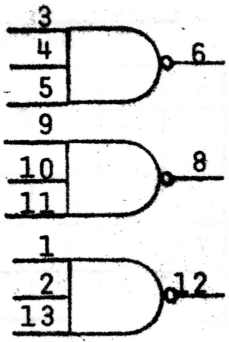
TRUTH TABLE

INPUTS		OUTPUT
1	2	3
0	0	0
0	1	0
1	0	0
1	1	1

VCC PIN 14

GND PIN 7

7410
TRIPLE 3-INPUT NAND GATE



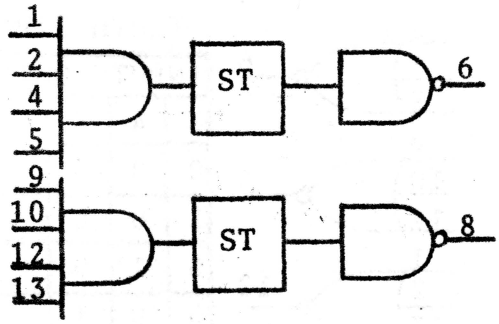
TRUTH TABLE

INPUTS			OUTPUT
3	4	5	6
0	0	0	1
1	0	0	0
0	1	0	0
0	0	1	0
1	1	1	0

VCC PIN 14

GND PIN 7

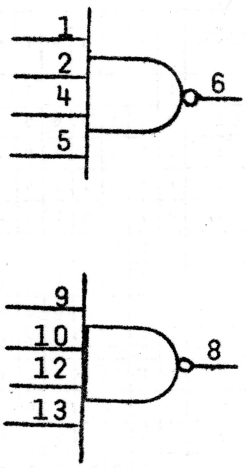
7413
DUAL NAND SCHMITT TRIGGER



VCC PIN 14

GND PIN 7

7420
DUAL 4-INPUT NAND GATE



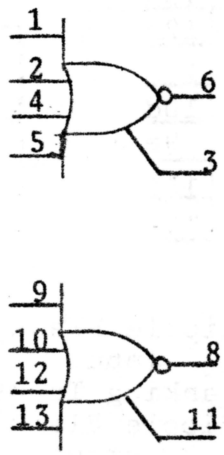
TRUTH TABLE

INPUTS				OUTPUT
1	2	4	5	6
0	0	0	0	1
1	0	0	0	1
0	1	0	0	1
0	0	1	0	1
0	0	0	1	1
1	1	1	1	0

VCC PIN 14

GND PIN 7

7425
DUAL 4-INPUT NOR WITH STROBE



TRUTH TABLE

INPUTS					OUTPUT
1	2	4	5	3	6
1	X	X	X	1	0
X	1	X	X	1	0
X	X	1	X	1	0
X	X	X	1	1	0
0	0	0	0	X	1
X	X	X	X	0	1

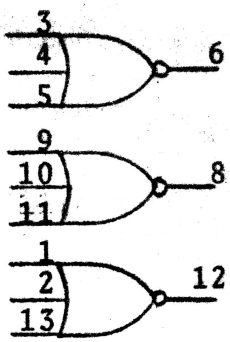
X=IRRELEVANT

VCC PIN 14

GND PIN 7

9670

7427
TRIPLE 3-INPUT NOR GATE



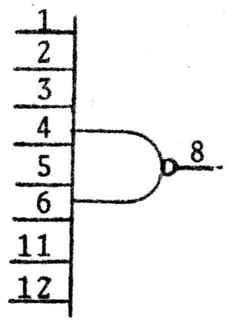
TRUTH TABLE

INPUTS			OUTPUT
3	4	5	6
0	0	0	1
1	0	0	0
0	1	0	0
0	0	1	0
1	1	1	0

VCC PIN 14

GND PIN 7

7430
SINGLE 8-INPUT NAND GATE



VCC PIN 14

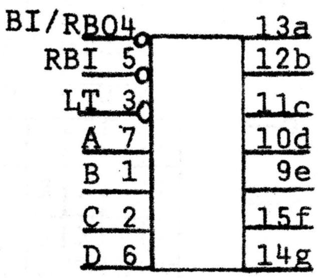
GND PIN 7

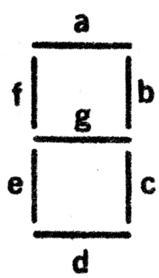
TRUTH TABLE

INPUTS								OUTPUT
1	2	3	4	5	6	11	12	8
0	X	X	X	X	X	X	X	1
X	0	X	X	X	X	X	X	1
X	X	0	X	X	X	X	X	1
X	X	X	0	X	X	X	X	1
X	X	X	X	0	X	X	X	1
X	X	X	X	X	0	X	X	1
X	X	X	X	X	X	0	X	1
X	X	X	X	X	X	X	0	1
1	1	1	1	1	1	1	1	0
0	0	0	0	0	0	0	0	1

X=IRRELEVANT

7448
BCD TO 7-SEGMENT DECODER





RBI= Ripple Blanking Input

BI= Blanking Input

RBO= Ripple Blanking Output

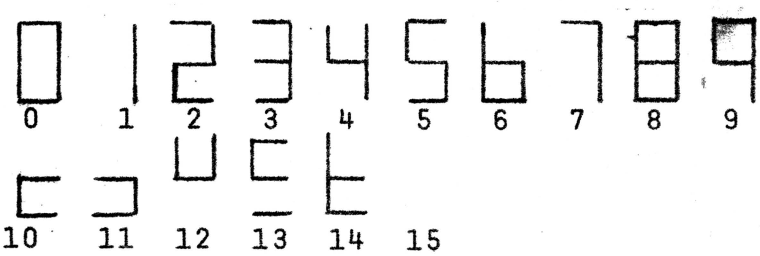
LT= Lamp Test

VCC PIN 16

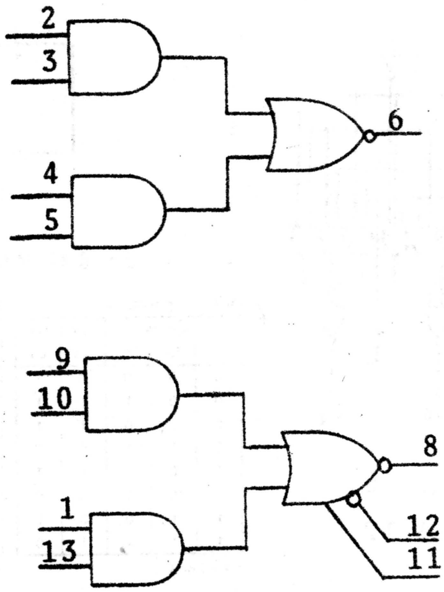
GND PIN 8

DECIMAL OR FUNCTION	INPUTS $\overline{LT}$	$\overline{RBI}$	D	C	B	A	$\overline{BI/RBO}$	OUTPUTS a	b	c	d	e	f	g	NOTE
0	1	1	0	0	0	0	1	1	1	1	1	1	1	0	1
1	1	X	0	0	0	1	1	0	1	1	0	0	0	0	1
2	1	X	0	0	1	0	1	1	1	0	1	1	0	1	
3	1	X	0	0	1	1	1	1	1	1	1	0	0	1	
4	1	X	0	1	0	0	1	0	1	1	0	0	1	1	
5	1	X	0	1	0	1	1	1	0	1	1	0	1	1	
6	1	X	0	1	1	0	1	0	0	1	1	1	1	1	
7	1	X	0	1	1	1	1	1	1	1	0	0	0	0	
8	1	X	1	0	0	0	1	1	1	1	1	1	1	1	
9	1	X	1	0	0	1	1	1	1	1	0	0	1	1	
10	1	X	1	0	1	0	1	0	0	0	1	1	0	1	
11	1	X	1	0	1	1	1	0	0	1	1	0	0	1	
12	1	X	1	1	0	0	1	0	1	0	0	0	1	1	
13	1	X	1	1	0	1	1	1	0	0	1	0	1	1	
14	1	X	1	1	1	0	1	0	0	0	1	1	1	1	
15	1	X	1	1	1	1	1	0	0	0	0	0	0	0	
$\overline{BI}$	X	X	X	X	X	X	0	0	0	0	0	0	0	0	2
$\overline{RBI}$	1	0	0	0	0	0	0	0	0	0	0	0	0	0	3
$\overline{LT}$	0	X	X	X	X	X	1	1	1	1	1	1	1	1	4

X=IRRELEVANT



7450
DUAL AND/OR GATE (INVERTER/EXPANDER)



TRUTH TABLE

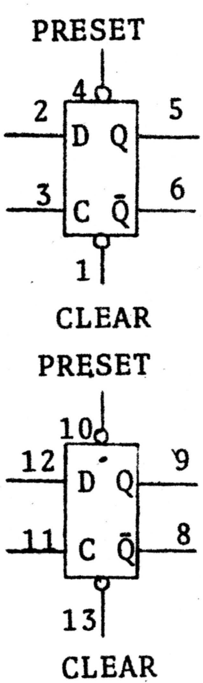
A	B	C	D	Y	
0	X	0	X	1	WHEN PIN 11 = 0
0	X	X	0	1	
X	0	0	X	1	
X	0	X	0	1	
1	1	X	X	0	
X	X	1	1	0	
X	X	X	X	0	WHEN PIN 11 = 1

$\boxed{X}$ = IRRELEVANT

X AND $\bar{X}$ MUST BE OPPOSITE STATES SIMULTANEOUSLY

VCC PIN 14
GND PIN 7

7474
DUAL D FLIP FLOP



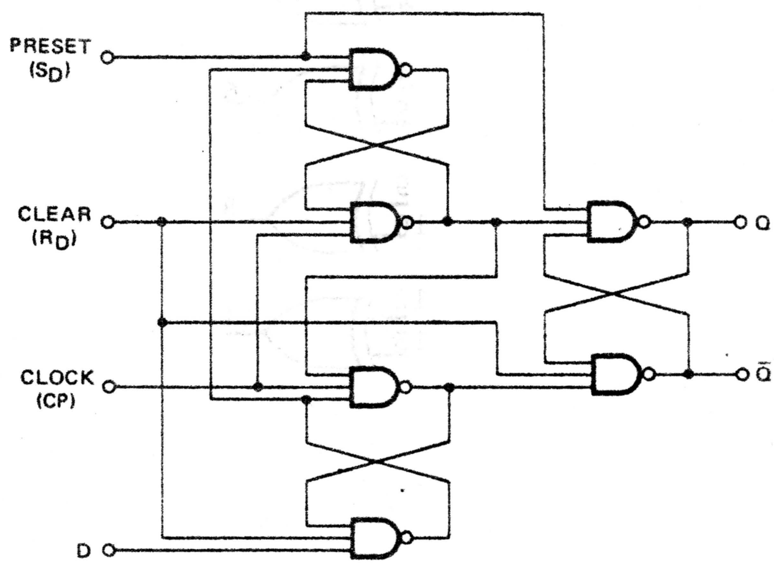
TRUTH TABLE (Each Flip-Flop)

t_n	t_{n+1}	
INPUT D	OUTPUT Q	OUTPUT $\bar{Q}$
L	L	H
H	H	L

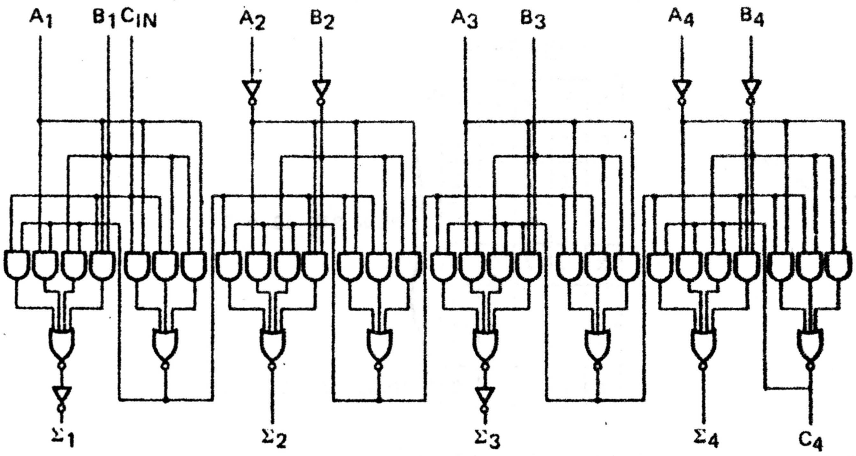
NOTES:
t_n = bit time before clock pulse.
t_{n+1} = bit time after clock pulse.

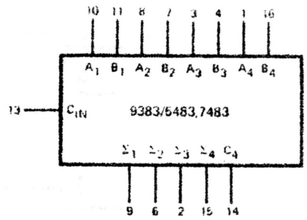
VCC PIN 14
GND PIN 7

LOGIC DIAGRAM (EACH FLIP-FLOP)



7483
4-BIT FULL ADDER





2-bit & 4-bit Adder Truth Table

ODD* bit positions:

INPUTS			OUTPUTS	
C_{x-1}	A_x	B_x	Σ_x	C_x
0	0	0	0	1
0	0	1	1	1
0	1	0	1	1
0	1	1	0	0
1	0	0	1	1
1	0	1	0	0
1	1	0	0	0
1	1	1	1	0

* X = 1 or 3

EVEN† bit positions:

INPUTS			OUTPUTS	
$\bar{C}_{x-1}$	A_x	B_x	Σ_x	C_x
1	0	0	0	0
1	0	1	1	0
1	1	0	1	0
1	1	1	0	1
0	0	0	1	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	1

† X = 2 or 4

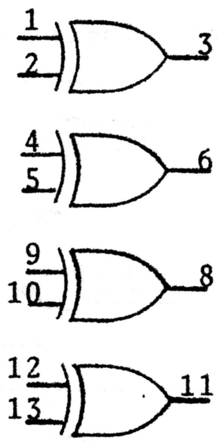
PIN NAMES

A_1, B_1, A_3, B_3	Data Inputs
A_2, B_2, A_4, B_4	Data Inputs
C_{IN}	Carry Input
$\Sigma_1, \Sigma_2, \Sigma_3, \Sigma_4$	Sum Outputs
C_4	Carry Out Bit 4

VCC PIN 5

GND PIN 12

7486
QUAD EXCLUSIVE OR GATE



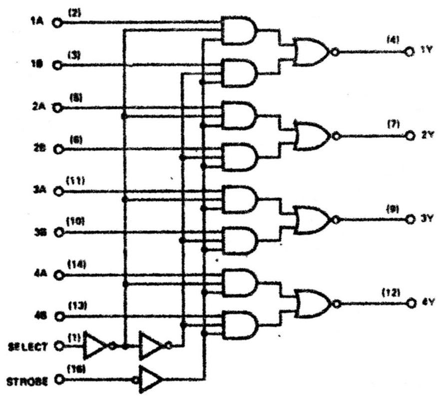
TRUTH TABLE

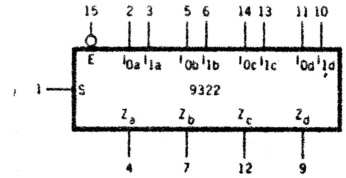
INPUTS		OUTPUT
1	2	3
0	0	0
1	0	1
0	1	1
1	1	0

VCC PIN 14

GND PIN 7

74157
QUAD 2-INPUT DATA SELECTOR/MULTIPLEXER



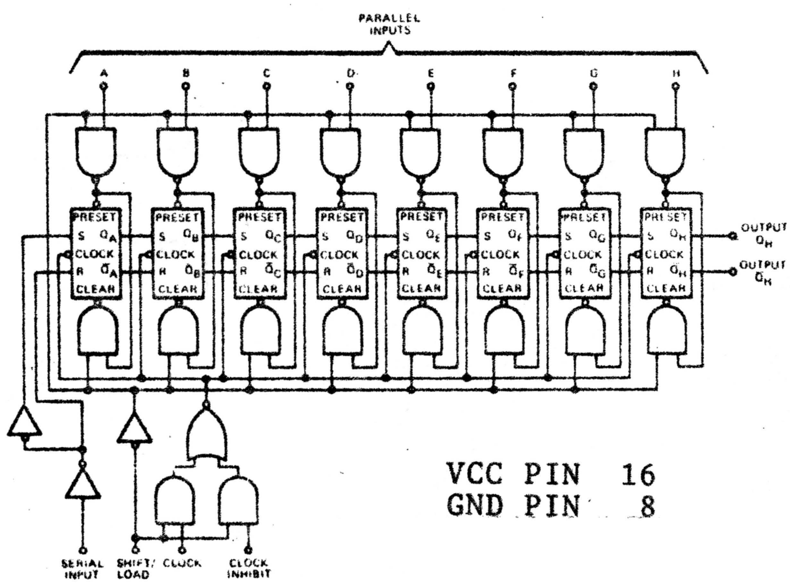


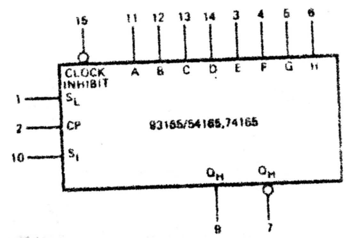
TRUTH TABLE

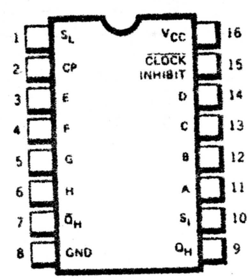
INPUTS			OUTPUT
STROBE	SELECT	A B	Y
H	X	X X	L
L	L	L X	L
L	L	H X	H
L	H	X L	L
L	H	X H	H

VCC PIN 5
GND PIN 12

74165
PARALLEL-LOAD 8-BIT SHIFT REGISTER

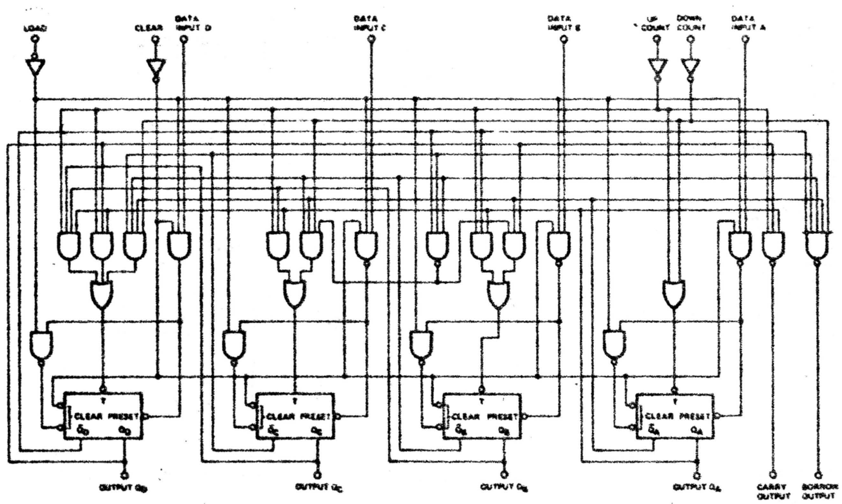


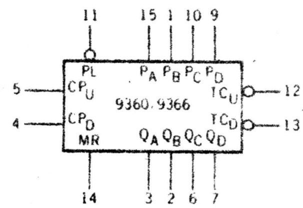


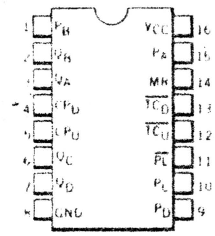


VCC PIN 16
GND PIN 8

74192
SYNCHRONOUS DECADE UP/DOWN COUNTER
74193
SYNCHRONOUS BINARY UP/DOWN COUNTER

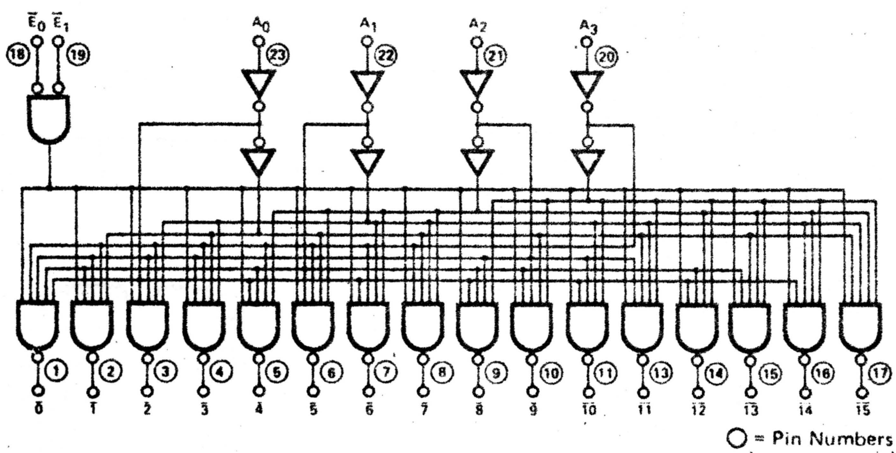


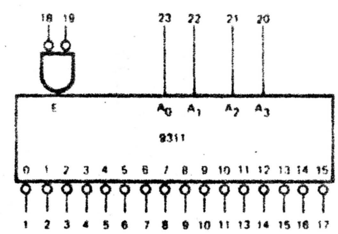


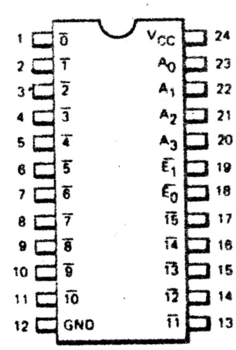


VCC PIN 16
GND PIN 8

9311
ONE-OF-SIXTEEN DECODER/DEMULTIPLEXER

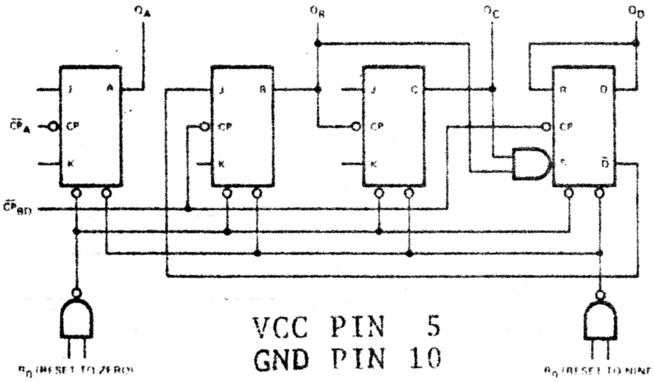






VCC PIN 12
GND PIN 24

7490
DECADE COUNTER

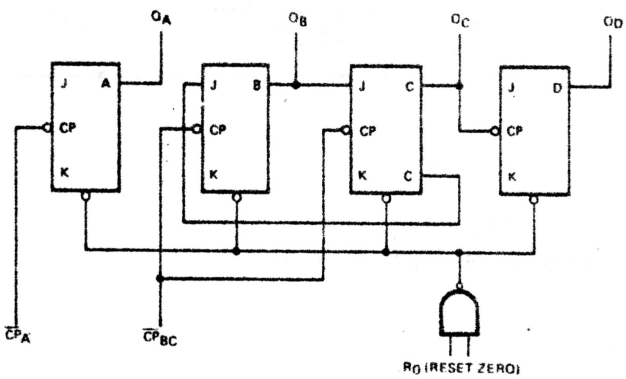


VCC PIN 5
GND PIN 10

TRUTH TABLE

COUNT	OUTPUT D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

7492
DIVIDE-BY-(2-6-12) COUNTER

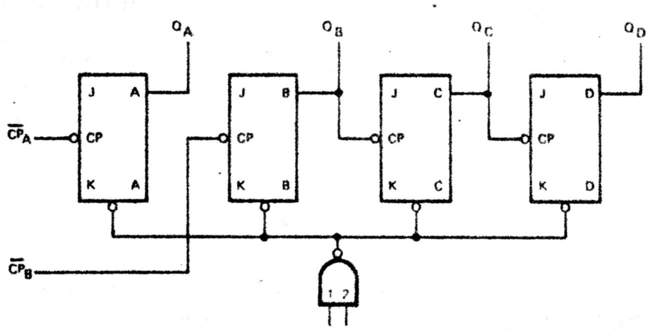


VCC PIN 5
GND PIN 10

TRUTH TABLE

COUNT	OUTPUT D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	1	0	0	0
7	1	0	0	1
8	1	0	1	0
9	1	0	1	1
10	1	1	0	0
11	1	1	0	1

7493
4-BIT BINARY COUNTER

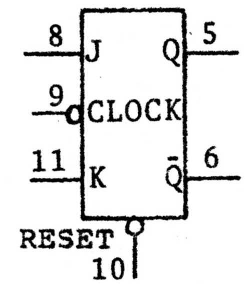


VCC PIN 5
GND PIN 10

TRUTH TABLE

COUNT	OUTPUT D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

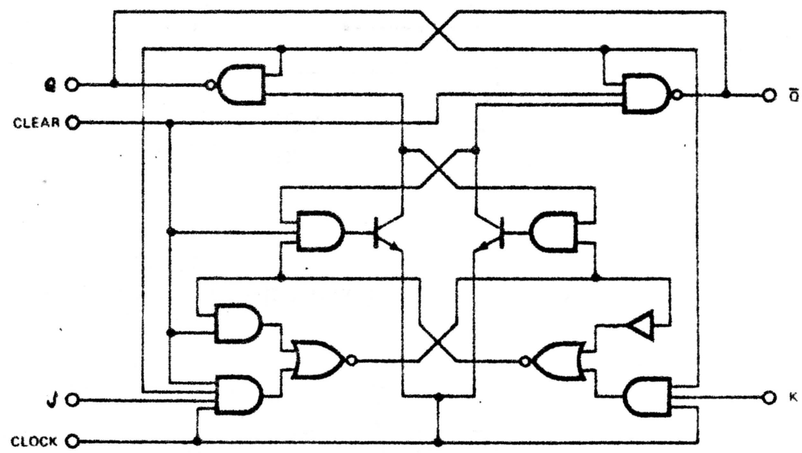
74107
DUAL JK M/S FLIP FLOP

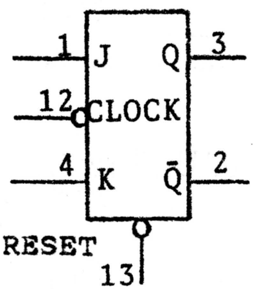


TRUTH TABLE

t_n		t_{n+1}
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\bar{Q}_n$

LOGIC DIAGRAM
(EACH FLIP-FLOP)

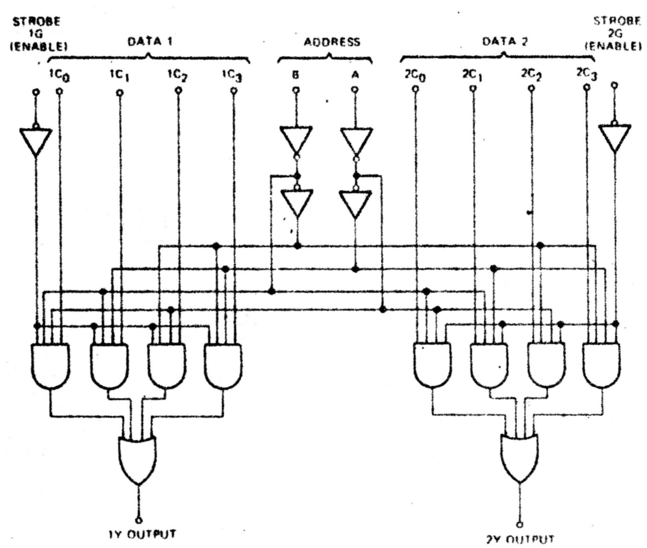


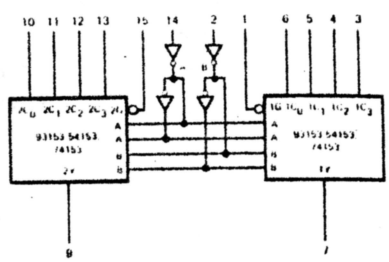


VCC PIN 16
GND PIN 8

NOTES:
t_n = Bit time before clock pulse.
t_{n+1} = Bit time after clock pulse.

74153
DUAL 4-BIT MULTIPLEXER

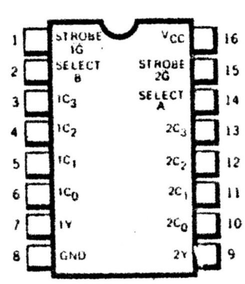




TRUTH TABLE

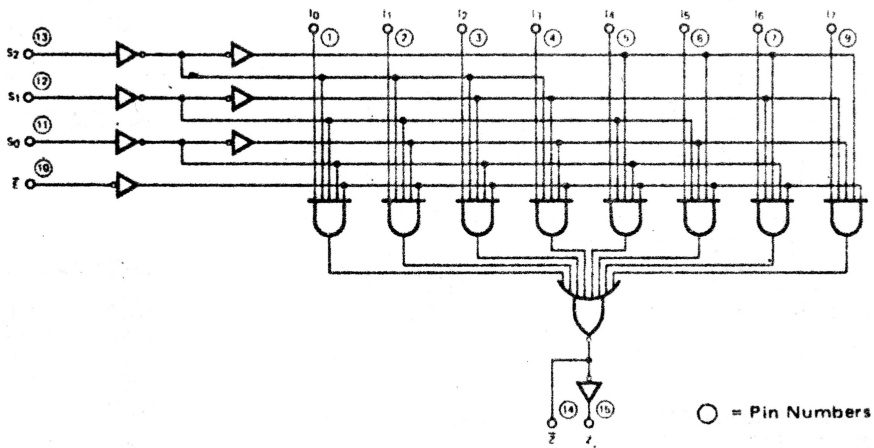
ADDRESS INPUTS		DATA INPUTS				STROBE	OUTPUT
B	A	C_0	C_1	C_2	C_3	G	Y
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

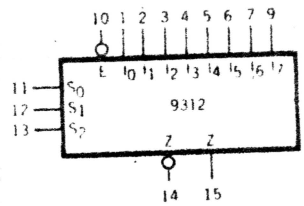
Address Inputs A and B are common to both sections
H = HIGH level, L = LOW level, X = irrelevant

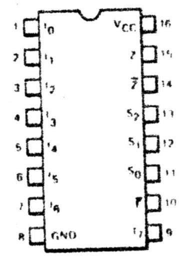


VCC PIN 16
GND PIN 8

9312
8-INPUT MULTIPLEXER







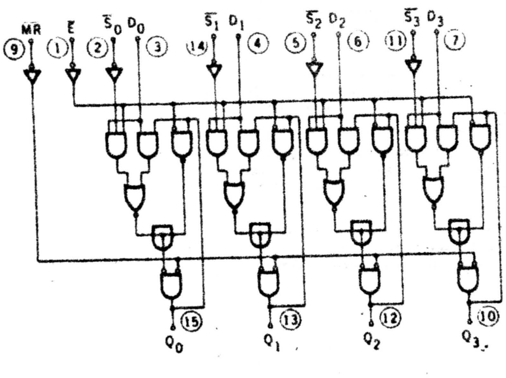
○ = Pin Numbers

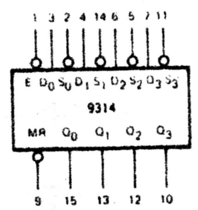
PIN NAMES

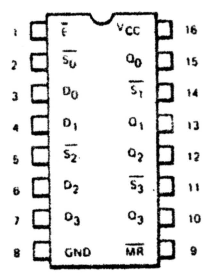
S_0, S_1, S_2	Select Inputs
$\overline{E}$	Enable (Active LOW) Input
I_0 to I_7	Multiplexer Inputs
Z	Multiplexer Output (Note b)
$\overline{Z}$	Complementary Multiplexer Output (Note b)

VCC PIN 16
GND PIN 8

9314
QUAD LATCH



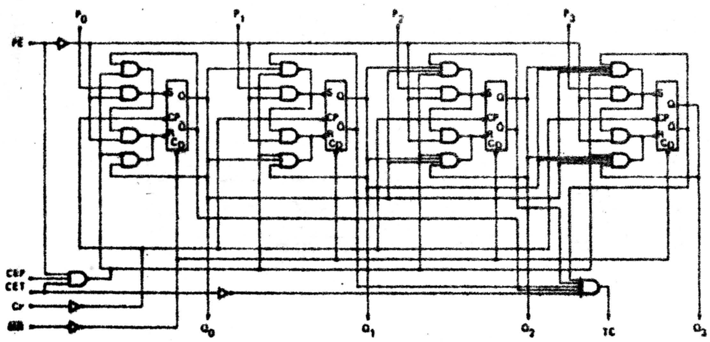


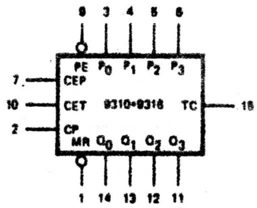


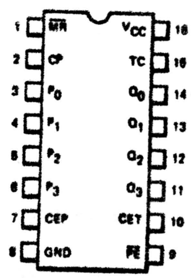
VCC PIN 16
GND PIN 8

9316
4-BIT BINARY COUNTER

9316







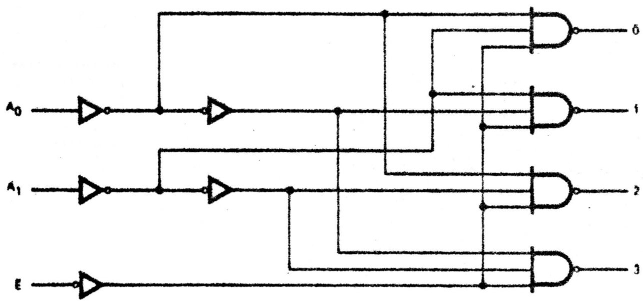
MODE SELECTION

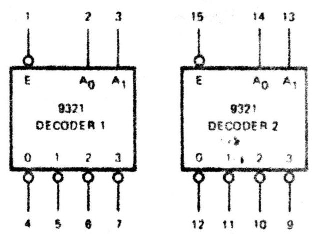
$\overline{PE}$	CEP	CET	MODE
L	L	L	Preset
L	L	H	Preset
L	H	L	Preset
L	H	H	Preset
H	L	L	No Change
H	L	H	No Change
H	H	L	No Change
H	H	H	Count

($\overline{MR}$ = HIGH)

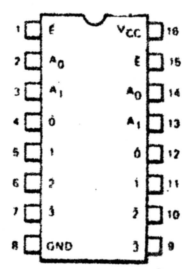
VCC PIN 16
GND PIN 8

9321
DUAL ONE-OF-FOUR DECODER

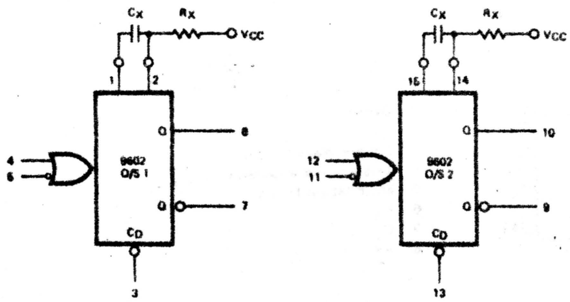


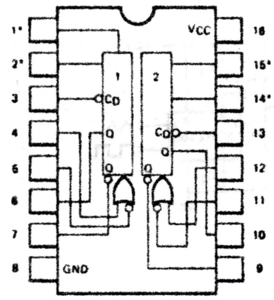


VCC PIN 16
GND PIN 8



9602
DUAL MONOSTABLE MULTIVIBRATOR





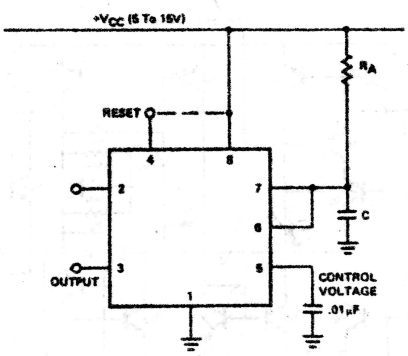
VCC PIN **16**
GND PIN 8

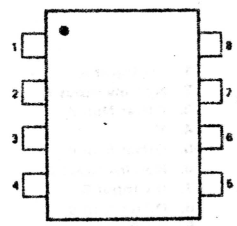
$$t = 0.31\, R_X C_X \left[1 + \frac{1}{R_X}\right]$$

Where R_X is in kΩ, C_X is in pF
t is in ns
for $C_X < 10^3$ pF

NE555
TIMER

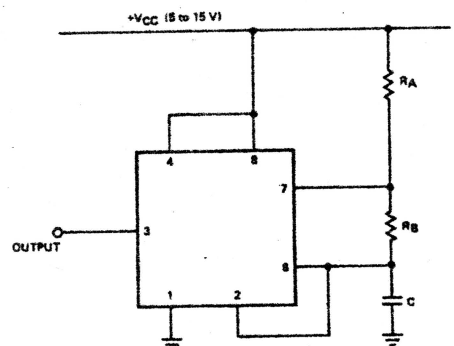
MONOSTABLE OPERATION



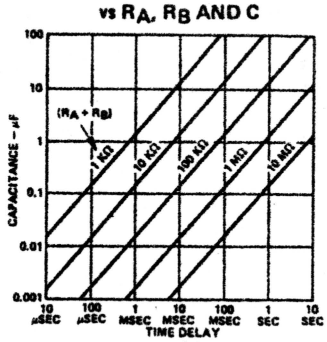


1. Ground
2. Trigger
3. Output
4. Reset
5. Control Voltage
6. Threshold
7. Discharge
8. V_{CC}

ASTABLE OPERATION



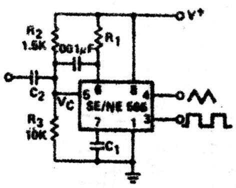
TIME DELAY vs R_A, R_B AND C

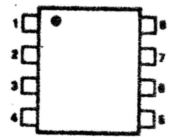


The duty cycle is given by:

$$D = \frac{R_B}{R_A + 2R_B}$$

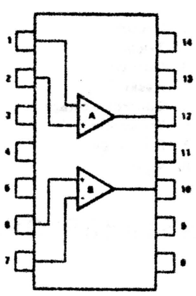
NE566
FUNCTION GENERATOR



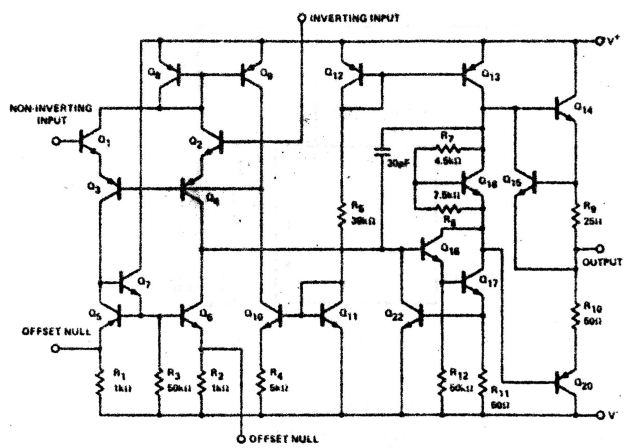


1 Ground
2 NC
3 Square Wave Output
4 Triangle Wave Output
5 Modulation Input
6 R_1
7 C_1
8 V+

747
DUAL OPERATIONAL AMPLIFIER



1. Inv Input A
2. Non-inv Input A
3. Offset Null A
4. V-
5. Offset Null B
6. Non-inv Input B
7. Inv Input B
8. Offset Null B
9. V+ B
10. Output B
11. No Connect
12. Output A
13. V+ A
14. Offset Null A



IC INTRODUCTION

The following section will inform the user of this handbook as to what to expect when testing an integrated circuit. We recommend that you correlate the logic levels typically found (i.e. 1, 0 or P) as: high being 2.4VDC to Vcc (supply voltage typically 5VDC); low being 0.0VDC; 0.8VDC pulsing being any change of state from high to low or low to high. For your convenience, the probes are color coded with lights to represent the logic states.

Red = 1 or high White = 0 or low
Blue = Pulsing or change of state

A typical example of the use of a probe as equated to the use of a truth table is as follows:

2 INPUT NOR

A	B	Y
0	0	1
1	0	0
0	1	0
1	1	0

A	B	Y
WHITE	WHITE	RED
RED	WHITE	WHITE
WHITE	RED	WHITE
RED	RED	WHITE

Consider now a complex device (i.e. an eight input nand gate 7430). If you were to continue a truth table using only ones (1s) and zeros (0s) and if you were to expand it out fully, you would have 40,320 data input bits. Therefore we need a method of abbreviating the truth table. You will note the three input nomenclatures for the following truth tables.

A - H	input gates
Y	output
$\overline{Y}$	inverted Y output
Q	flip-flop output
$\overline{Q}$	inverted Q output
X	irrelevant (any state)

The X nomenclature indicates that any signal level may be present at that gate at that time and it will not affect the output condition of the device. That is, because the other inputs are set in a particular fashion, the change of state will not affect it.

I.C. LOGIC DESIGN (LDP-1B)

The I.C. Logic Design Program (LDP-1B) is ideal for engineers and technicians who are beginning to design, test, or repair equipment using I.C.'s. The course is based on working with standard I.C. logic devices as they are offered by manufacturers.

Completion of the course will enable the student to operate effectively when designing or analyzing. An outline of the lessons follows.

1. Logic Elements: This beginning lesson covers the AND, OR and inverter gates. Also included is a discussion of symbolic notation.
2. I.C. Logic Families: A study of each of the popular logic families including RTL, DTL, TTL, and ECL.
3. Complex Logic Elements: The student is taught the operational logic of standard packages containing more than one logic function. NAND, NOR, AND-OR-Invert and exclusive OR are covered. Also, Negative logic is studied.
4. Boolean Algebra & Theorems: Boolean Identities are taught. Also incluced are the theroems required to minimize logic circuits.
5. DeMorgan Theorem of Negation: This important theorem is taught in detail. Many practical examples are given.
6. Karnaugh Maps: This lesson teaches the student to minimize and graphically represent any logic circuit.
7. R/S Flip-Flops: The basic memory circuit is taught and its Truth Table studied. Included is the clocked R/S and Master-Slave.
8. Type D Flip-Flop: A study of the Type D and the Master-Slave Type D. The Truth Table is developed and studied.
9. JK Flip-Flop: This lesson teaches the student the operation of the Master-Slave JK Flip-Flop.
10. Pulse Forming Circuits: The student is taught to design bounce elimination circuits, one-shots, squaring circuits and a free running multivibrator using I.C. logic elements.

DIGITAL CIRCUIT DESIGN (DDP-1B)

This course covers the entire family of digital circuits; gates, flip-flops and trigger circuits. The unique format used in the text has the student designing complex circuits from basic building blocks. An emphasis has been placed on wave-forms and how they are generated by each circuit.

When finished with the DDP-1B the student will be able to design or troubleshoot any digital circuit using transistors or I.C.'s. An outline of the lessons follows.

1. Transistor Action: A study of alpha (d) and beta (p). Common Biasing techniques and DC analysis are included.
2. Semiconductor Diodes: A graphic study of the operation of diodes when forward and reverse biased. The effects of temperature and thermal derating are also covered.
3. Transistor Switching: This lesson includes the study of load lines, and DC switching parameters as they relate to transistor data sheets. Also a model of a transistor is developed. Use of the model simplifies the understanding of switching circuits.
4. Inverters: A step-voltage waveform, inversion, the transistor inverter and thermal derating are taught in this lesson. A design procedure and example are given.
5. Emitter Followers: A study of the operation of an emitter-follower circuit is given. Collector dissipation is included. A design procedure and example are given.
6. Diode Gates: Covers circuits using diodes as AND and OR gates. Truth Tables are also studied. A design procedure and example are given.
7. Diode-Transistor Gates: In this lesson the student is taught how to design logic gates using diodes and transistors as circuit elements. A design procedure and example are given.
8. Resistor-Transistor Gates: The student learns how to design a logic gate using resistors and transistors as circuit elements. A design procedure and example are given.
9. NAND/NOR Gates: The design of logic gating circuits using transistors connected in series and parallel is taught. A design procedure and example are given.
10. S/R Flip-Flops: A pulse waveform is studied in detail. Also the design of a set-reset flip-flop is taught. A design procedure and example are given.
11. Bistable Flip-Flops: Differentiation networks, commutating capacitors and bi-stable circuits are taught. A design example and procedure are given.
12. Astable Flip-Flops: The square-wave waveform is studied. The design of an astable flip-flop is taught. A design example and procedure are given.
13. Monostable Flip-Flop: The design of a "one-shot" is taught. A design procedure and example are given.
14. Schmitt Trigger Circuits: This lesson teaches the student to design trigger circuits having a specific UTP and LTP. A design procedure and example are given.

Kurz-Kasch, Inc.

Electronics Division
1421 S. Broadway
Dayton, Ohio 45401

Preliminary Product
Specification Sheet No.

HL-582

Model No. HL-582

User Price . . . $89.00

AN IN-CIRCUIT STIMULATOR TO EXERCISE ANY IC, CARD, OR SYSTEM IN QUESTION

By merely pressing the switch once, the HL-582 will pull an existing Lo state to a Hi state, an existing Hi state to a Lo state. The pulser is designed for use with DTL and TTL logic circuits. It may be applied to any input or output pulling them high and low. Noting the change in output (or lack of change) will identify troublesome circuits.

The high source and sink current capability overrides IC output points, originally in the Hi or Lo state. Duration of state change is approximately 1 μ Sec. A two-mode switch selects single cycle or 5 Hz repetition rate in continuous mode. Output is high, low or off (a high z state).

MODEL HL-582

Specifications

Pulse Voltage:	High level	3.0V min.
	Low level	0.6V max.
Pulse Width:	1 μ Sec. nominal (in both one-shot and continuous modes)	

PRF is 5 Hz/Sec. in continuous mode.

Power is derived from system under test (5.0V).

Power leads are overvoltage and reverse voltage protected.

Tip protected to ± 35 volts.

Telephone 513/296-0330

Kurz-Kasch 500 Series Logic Probes

New options
Improved features
Better specs

...complete logic systems analysis

Rugged, all solid-state, Kurz-Kasch logic probes are designed for fast, accurate testing of logic levels in all types of integrated circuit systems. A simple readout system indicates "one," "zero" or "pulse" readings precisely through color-coded visual electronic readouts in the probe tip. Absence of logic levels is indicated by all readouts remaining OFF.

All units are rugged, solid-state instruments in attractive chrome-finished steel cases. High input impedance at the Logic "1" level prevents loading of the circuit under test. Power is derived from the equipment being tested.

Use logic probes for field service, inspection, monitoring, production line checkout, or engineering lab circuit designing.

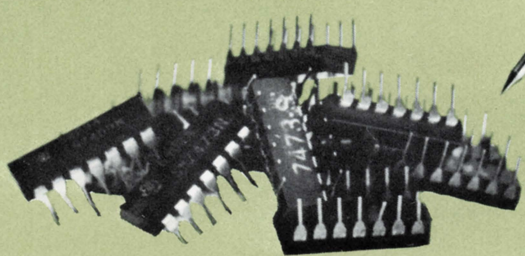
applications

Logic levels can be accurately tested in virtually any (DTL, TTL) IC system including desk calculators, business machines, N/C devices, computers or telephone systems. Power is derived from the unit under test allowing use in the field or in the lab. A must item for every digital field serviceman.

specifications

Readout Light Red = Logic "1"
Readout Light White = Logic "0"
No Readout Light = "infinity"
Readout Light Blue = "pulse"

High input impedance prevents loading of circuit under test. Size 9/16″ dia., 6″ long, 26¾″ leads with clip-on terminals.

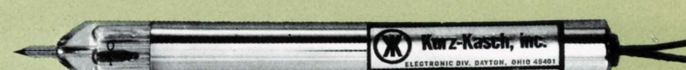


A pulse detection feature is available on most models of logic probe. A third readout is provided to display high speed pulse trains or a single cycle pulse of 50 nanoseconds or greater on the standard Model LP-520. Overvoltage protection to ±100 volts DC intermittent. Power lead reversal protection is standard on all models.

add these options:

G-S-M: Gating Feature (-G)— 3 Channel input for timing. Pulse indicator displays only when probe tip and gate/gates are in coincidence. **Memory & Stretch (-M)**— Push-pull switch for selecting stretch or latch mode. Stretch mode detects high speed pulse and displays blue "P" lamp for 200 mS. Latch mode captures high speed pulse/trains and latches blue "P" on until reset. **5 Nano-second capability (-S)**— Allows detection of pulses up to 10 x faster than standard probes. Each option $10.00.

Logic Probe Model LP-510 for 4.75-5.5 V DC Logic Systems Overload Protected



Overvoltage protection prevents damage to the probe circuits if the probe tip accidentally touches voltages other than the logic level source. Overvoltage protection on the Model LP-510 input is to ±100 V DC intermittent.

Power lead reversal protection. If power leads are accidentally connected in reverse, the probe is self-protected.

specifications

Probe Power Requirements: 4.75 to 5.5 vdc

Voltage: all logic voltage levels from 4.75 vdc to Vc compatible with DTL, TTL and similar families

Note: Overvoltage input protection to ±100 vdc, intermittent

Input Impedance: greater than 35K ohms for logic "1" level

Logic Voltage Level Response: 0-0.8 vdc = logic "0" readout (white) at tip
0.8-2.4 vdc = no readout
2.4-Vc = logic "1" readout (red) at tip
No readout in case of missing pin or unconnected wire

Size: 9/16″ dia., 6″ long, 26¾″ leads with clip-on terminals. Price $44.95

Kurz-Kasch, Inc.
ELECTRONICS DIVISION
2876 Culver Avenue
Dayton, Ohio 45429
Telephone 513/296-0330

Logic Probe Model LP-520 For Complete Advanced Testing of 4.75-5.5 V DC Logic

This advanced Model LP-520 offers complete logic analysis capability, input overload protection, plus high speed pulse detection with separate readout, and power lead reversal protection.

Three color-coded readouts located at the probe tip for fast, easy testing. Pulse readout illuminates to display high speed pulse trains, or single cycle (− or +) pulse of 50 nanoseconds duration or greater. LP-520 is the only test instrument that will perform all necessary IC Logic test functions at an economical price.

Even more useful with G-S&M options. See front.

specifications

Probe Power Requirements: 4.75 to 5.5 vdc

Voltage: all logic voltage from 4.75 vdc to Vc compatible with DTL, TTL and similar families

Note: Overvoltage input protection to ±100 vdc, intermittent.

Input Impedance: greater than 35K ohms for logic "1" level

Logic Voltage Level Response: 0-0.8 vdc = logic "0" readout (white) at tip
0.8-2.4 vdc = no readout 2.4-Vc = logic "1" readout (red) at tip
No readout in case of missing pin or unconnected wire

Pulse Detection Response: high-speed pulse trains, or single cycle (negative or positive pulse of 50 nanoseconds duration or greater) = blue readout at tip. Pulse stretcher remains on for 200 milliseconds

Size: 9/16″ dia., 6″ long, 26¾″ leads with clip-on terminals. Price $69.95

Logic Probe Model LP-530 For Advanced Testing of 12-15 V DC Logic

Overvoltage protection prevents damage to the probe circuits if the probe tip accidentally touches voltages other than the logic level source. Overvoltage protection on the Model LP-530 input is to ±100 V DC intermittent.

Power lead reversal protection. If power leads are accidentally connected in reverse, the probe is self protected. For use with 12-15 V DC logic circuits.

specifications

Probe Power Requirements: 12 to 15 vdc

Voltage: all logic voltage levels in the 12-15 vdc range compatible with DTL, TTL and similar families

Note: Overvoltage input protection to ±100 vdc, intermittent.

Input Impedance: greater than 100,000 ohms for logic "1" level

Logic Voltage Level Response: 0-1.5 vdc = logic "0" readout (white) at tip
1.5-10 vdc = no readout
10-Vc = logic "1" readout (red) at tip
No readout in case of missing pin or unconnected wire

Size: 9/16″ dia., 6″ long, 26¾″ leads with clip-on terminals. Price $44.95

Logic Probe Model LP-540 For Complete Advanced Testing of 12-15 V DC Logic

This advanced Model LP-540 offers complete logic analysis capability, input overload protection, plus high speed pulse detection with separate readout and power lead reversal protection.

Three color-coded readouts located at the probe tip for fast, easy testing. Pulse readout illuminates to display high speed pulse trains, or single cycle (− or +) pulse of 50 nanoseconds duration or greater. LP-540 is the only test instrument that will perform all necessary IC logic test functions at an economical price.

specifications

Probe Power Requirements: 12 to 15 V DC

Voltage: all logic voltage levels in the 12-15 V DC range compatible with DTL, TTL and similar families

Note: Overvoltage input protection to ±100 vdc, intermittent.

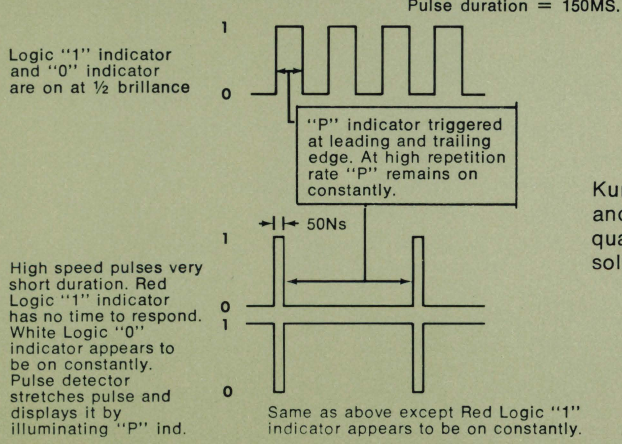
Input Impedance: greater than 100,000 ohms for logic "1" level

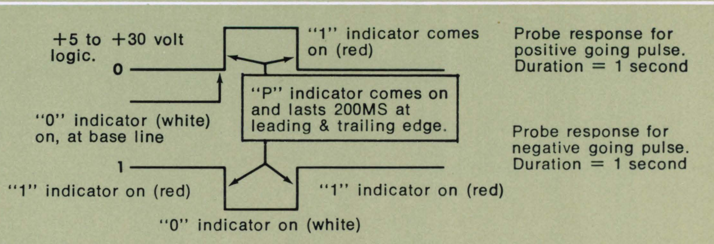
Logic Voltage Level Response: 0-1.5 vdc = logic "0" readout (white) at tip
1.5-10 vdc = no readout 10-Vc = logic "1" readout (red) at tip
No readout in case of missing pin or unconnected wire

Pulse Detection Response: high-speed pulse trains, or single cycle (negative or positive pulse, of 50 nanoseconds duration or greater)= blue readout at tip. Pulse stretcher remains on for approximately 200 milliseconds

Size: 9/16″ dia., 6″ long, 26¾″ leads with clip-on terminals. Price $69.95

LOGIC PROBE RESPONSE FOR GIVEN INPUT CONDITIONS.





Kurz-Kasch logic probes provide all the information you need to quickly and accurately evaluate all logic systems . . . and they are the highest quality, most economical logic testing instruments available. Call our problem solving engineers today for complete details on special logic probes -

*Patent #3,525,939 applies, others pending

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Dayton, Ohio 45429
Telephone 513/296-0330

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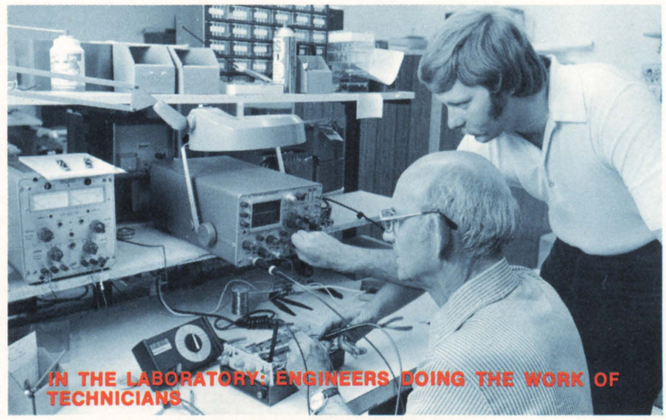
Litho in U.S.A.

WE KNOW WHAT YOUR TROUBLE-SHOOTING PROBLEMS ARE AND WE'RE DOING SOMETHING ABOUT IT!


PLANT MAINTENANCE: PRODUCTION DELAYS DUE TO LENGTHY SET-UP AND REPAIR TIME


IN THE LABORATORY: ENGINEERS DOING THE WORK OF TECHNICIANS


ON THE LINE: MISSED SHIPPING DATES DUE TO FAULTY PC BOARDS


FIELD SERVICE: DISSATISFIED CUSTOMERS BECAUSE OF LENGTHY DOWN TIME

HERE'S

F.A.C.T.™

(FAILURE ANALYSIS BY COLOR TRACING)

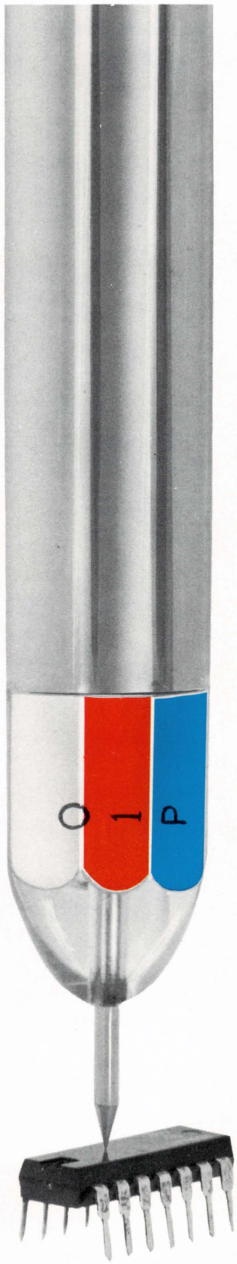
Digital Trouble-Shooting System

HERE'S HOW F.A.C.T.™ WORKS!

It all started in the early '60's . . .
The advent of digital circuits in the early '60's created an idea that trouble-shooting would be simple and easy. People commonly talked about 1's and 0's. Most of the circuits used in equipment were made up of discreet devices of limited capability. This was due to size and cost. As a result, this equipment was easier to understand and maintain in comparison to today's IC based equipment. Trouble shooting was aimed at finding a bad transistor, diode, etc. The oscilloscope not only made sense, but was the only practical device available for trouble-shooting. However, while the transition to digital circuits was in progress, scopes remained essentially analog test equipment.

Changes occurred in the middle '60's . . .
Integrated circuits gained popularity. Equipment did not become smaller as expected. Instead, equipment became more complex. The same size machine did more and faster. Increased machine capability required greater in-depth knowledge of circuit operations. Unfortunately, analog test equipment (scopes and meters) became less efficient because circuit analysis is virtually impossible and definitely impractical on such test equipment. Imagine trying to analyze a circuit with hundreds or thousands of IC's (including today's MSI devices such as adders, up-down counters, etc.).

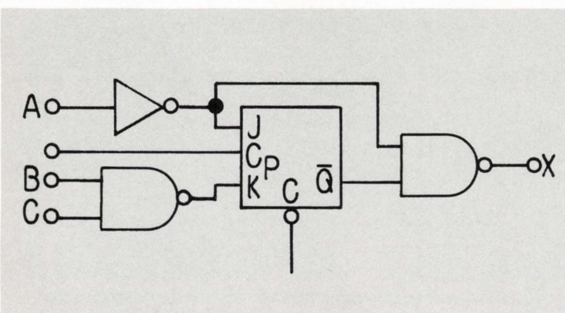
Enter the age of the Logic Probe . . .
In the late '60's, Kurz-Kasch developed the highly sophisticated and inexpensive Logic Probe. This 3-lamp device gives answers. In fact, it gives more answers at any given point in a circuit than you can get from a $2500 scope. While the scope displays logic 1's, 0's and circuit transitions; the Logic Probe indicates all of this information plus open circuits and incorrect logic levels. This advantage was possible to achieve because of the standardization of logic levels (TTL/DTL 5V), (HTL 12-15V), etc. This opened the door to a better idea; Kurz-Kasch Logic Probes with multiple lamp readouts. Not only does the logic probe provide more information; it does not require costly calibration and lengthy set-up time. Just hook up the clip leads and begin trouble shooting at once.



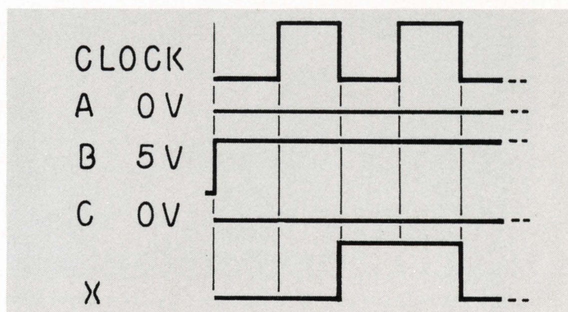
Kurz-Kasch keeps pace in the '70's . . .
Recognizing the need for simpler, faster and less expensive methods of repair and installation of today's complex equipment, Kurz-Kasch engineers invested six months in the field discussing trouble-shooting problems with customers and field service technicians. As a result of this study, a revolutionary new method of simplified trouble shooting is being introduced. Basically, all trouble-shooting is a comparison (that is observing what is happening in a circuit and comparing it to what should be happening). Because Kurz-Kasch Logic probes are faster than scopes, meters, clips and comparitors; Kurz-Kasch Logic Probes are without a doubt the most inexpensive and effective test equipment available. Also Kurz-Kasch Logic Probes are convenient (can be carried in a shirt pocket). With this excellent system of test equipment, Kurz-Kasch now introduces F.A.C.T.!

What is F.A.C.T.?
F.A.C.T. (Failure Analysis by Color Tracing) is a revolutionary new system developed by Kurz-Kasch Electronic Division in conjunction with their multiple display Logic Probes and Pulsers.

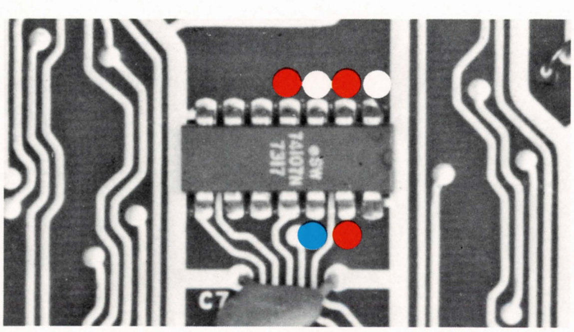
What does F.A.C.T. do?
F.A.C.T. offers you the fastest comparison possible; that of color tracing. Just compare the color observed at a given point with the color marked on a print, schematic or overlay . . . and if it agrees; there's no fault. F.A.C.T. is in fact, a simple solution to a complex problem. F.A.C.T. gives a new perspective to the training requirements needed to make a field engineer proficient with a new piece of equipment.



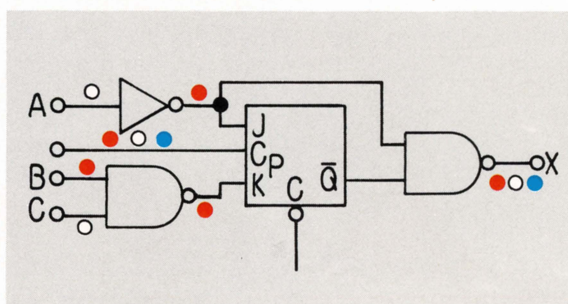
Simple circuit diagram using JK Flip-Flops and some gates.



Simple, but complex waveforms in time relationships which must be known by the technician. Conventional test equipment needed to determine waveform analysis would require lengthy set up time and calibration.



1. Color overlay on P.C. Board — By using F.A.C.T.; Real time color displays eliminates set-up time and reduces the need for understanding circuits.



2. Color Tracing on Wiring Diagram — Just compare color dots on stuffing diagram or schematic and compare logic points with the Kurz-Kasch Logic Probe. F.A.C.T. simplifies your field service problems.

3. Or simply write out the color F.A.C.T. listing on a note pad.

Facts about F.A.C.T.!

F.A.C.T. plus Logic Probes provides Real Time Testing!

You can believe what you see. Nothing gives as much information as the Logic Probe. Logic Probes work on either side of the PC board as well as on back planes. You can use F.A.C.T. systems anywhere in the equipment.

F.A.C.T. provides more information per Logic Point!

No other device, hand held or otherwise displays as much information as the Kurz-Kasch Logic Probes.

F.A.C.T. offers the fastest trouble shooting system available!

F.A.C.T. plus Logic Probes is faster than scopes, meters, clips, comparitors, etc. because you need not make decisions. The Logic Probe makes decisions for you and no set-up time is required.

F.A.C.T. and Logic Probes allow static and dynamic circuit testing!

With F.A.C.T. and Logic Probes, you can go through a static logic circuit, pulse the circuit and watch the action occur. Dynamic circuit testing is equally as simple.

F.A.C.T. plus Logic Probes is the LOWEST COST Test Equipment System!

Anyone from the Design Lab, Production Line, Plant Maintenance or Field Service can correlate the color system of F.A.C.T. to tracings or overlays. The only additional cost is the inexpensive Logic Probes (and the Hi-Lo Pulser, if desired).

F.A.C.T. relieves documentation worries!

It's simple to use F.A.C.T. Take a good board that is operating; mark up a stuffing diagram or schematic with corresponding color dots (as indicated by a Kurz-Kasch Logic Probe). Now you're ready to trouble-shoot a problem board on site.

F.A.C.T. reduces urgency in training!

Essentially, the Logic Probe knows more about each logic family than technicians. Logic Probes make decisions. Therefore, field service training is reduced to a minimum. With libraries of F.A.C.T., the urgency in training is eliminated.

No set-up time is required when you use F.A.C.T. and Logic Probes!

Conventional test equipment requires expensive set-up time. Many channels, synchronous arrangements and triggering requires a minimum of 20 minutes set-up time. With F.A.C.T. and Logic Probes, hook up the clip leads and begin testing.

How can YOU develop a F.A.C.T. System?

Simply check out a good board with a Kurz-Kasch Logic Probe observing the color displays, then mark up a print, schematic or overlay. Then simply compare. An overview of the equipment along with your F.A.C.T. analysis replaces block by block, circuit by circuit training. Documentation needs no longer be a nightmare to the technicians in the future. Field update is remarkably easy with F.A.C.T. F.A.C.T. employs inexpensive Kurz-Kasch Logic Probes without complicated interpretation or confusing interpolation on a Real Time Basis. Training time is reduced to a minimum because intimate circuit knowledge is not necessary. Technician competence is increased because of F.A.C.T.'s simplicity. The most important element of F.A.C.T. is that faster repair or installation provides less downtime and happier customers for you. Kurz-Kasch thinks this is what field service is all about!

LOGIC NODE ANALYSIS is possible with F.A.C.T.!

By using the Kurz-Kasch Logic Probe and Pulser combination, dynamic testing of any logic node is possible. You can check gates, flip-flops and registers. You can find unterminated inputs, solder bridges, open solder connections, no power on the board, open Vcc connections and lots more. You can use the probe to determine trigger levels or threshold levels with RC time constants in gates, multivibrator circuits, one shots, astables. Simply connect the pulser to input and the probe to output. The pulser automatically exercises the input node . . . if high the pulser will change the state to low, if low the pulser will change the state to high. By observing the color displays, the technician can determine if the chip is operating properly or needs replacement.

F.A.C.T. can be used by everyone!

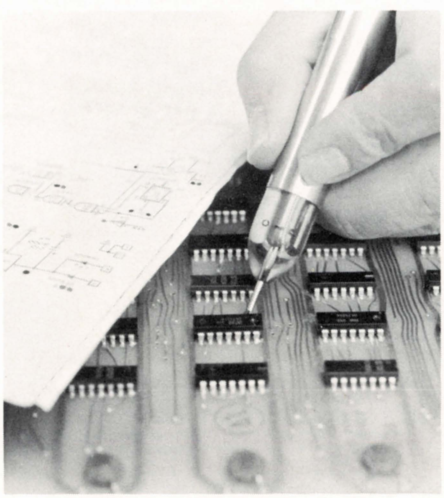
In the design lab: When designing a system, (to speed up prototyping) the design engineer wants to utilize the smallest decoupling capacitors. He also wants to use the minimum number of these components on the board. The Logic Probe helps the designer make decisions regarding IC's. Decisions which can be made no other way than by trial and error.

On the production line: Here documentation is the major problem. Equipment will hit the production floor with one foot in the design lab. Often there are many modifications ahead of documentation. By making overlays and comparing Logic Probe readouts, results are phenominal. F.A.C.T. makes sense to production people, QC and testing personnel.

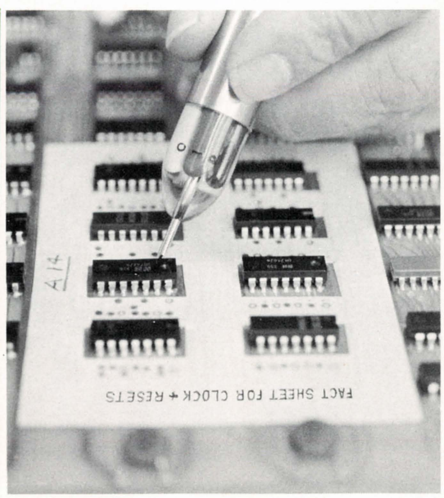
In Plant maintenance: Color trace a good board that is operating with the Logic Probe. Corresponding color tracings on overlays, stuffing diagrams or schematics provides plant maintenance personnel with a library of F.A.C.T. Compare F.A.C.T. to the faulty board and find the problem fast.

Field service at customer location: Installation and repair technicians don't have enough time to learn all about complex equipment. Their job is to repair and install quickly. F.A.C.T. relieves the urgency for training. Field service people don't have to understand the circuit . . . just compare Logic Probe displays and use F.A.C.T.

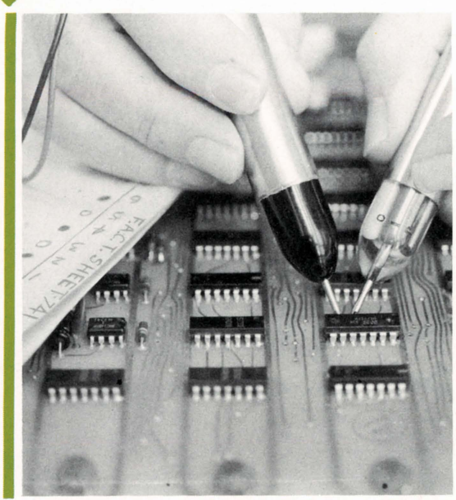
F.A.C.T.™ IN ACTION!



1. ELIMINATES INTERPRETATION OF LOGIC FUNCTIONS AND/OR COMPLEX WAVEFORMS — Simply compare colored tracings on a logic diagram to those displayed at the tip of the Logic Probe.

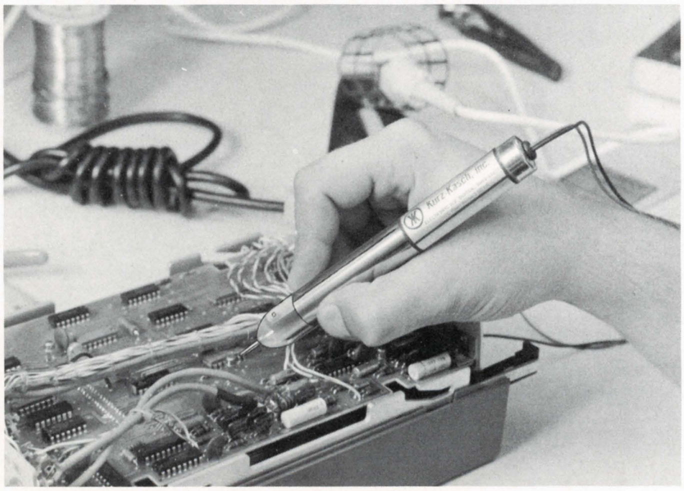


2. ELIMINATES DOCUMENTATION WORRIES— Make an overlay from an operating board, then record proper color displays to each pin as indicated by a Logic Probe — quickly find the faulty node by color tracing.



3. F.A.C.T. FINDS THE FAULTY NODE — Technicians can quickly and easily find the failure by exercising inputs with the HL582 Pulser and checking the output with the LP520 Logic Probe.

SIMPLIFY YOUR TROUBLE-SHOOTING PROBLEMS WITH KURZ-KASCH LOGIC PROBES AND F.A.C.T!



Here are the general features of Kurz-Kash Logic Probes:

1. Logic probes make decisions (Red, White, Hi/Lo pulse indicators will not light unless there are guaranteed logic highs and lows for the logic family being tested.
2. Logic probes indicate open pins or improper logic levels.
3. Logic probes provide fast pulse response plus stretched pulse for easy detection.
4. Logic probes determines polarity of pulse.
5. Logic probes provide unambiguous readout. No guessing as with some displays which are limited by too few readouts to display all the necessary information.
6. Duty cycle information is available up to the highest frequency of TTL. Kurz-Kasch Logic Probes indicate pulses and their polarity as well as indicating the duty cycle from 50% to 10 to 1 (all from DC to the limits of the IC's).
7. Logic probes are overvoltage protected at the tip and on the power line. Power leads are reverse voltage protected.
8. Your own Return on Investment study will indicate savings in thousands of dollars per man!

Choose the Kurz-Kasch Logic Probe that best suits your requirements:

LP510, LP520 Logic Probes: completely compatible with 5VDTL/TTL logic; LP520 Options: Gating, Memory and Speed options in any combination.

LP530, LP540 Logic Probes: completely compatible with 12-15V HTL logic: LP 540 Options: Gating, Memory and Speed options in any combination.

LP560 Logic Probes: completely compatible with RTL logic: Options: Memory and Gating options.

LP575, LP576 Logic Probes: completely compatible with 5-15V C/MOS and 12-15V HTL logic. Options: Memory option.

LG580: 5V square wave generator

LG581: 12-15V square wave generator

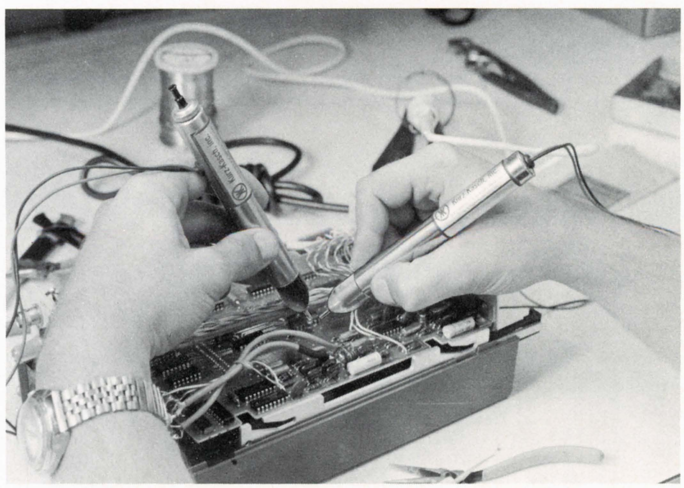
Take advantage of our 30 DAY FREE TRIAL OFFER, Try one!

Let Kurz-Kasch Logic Probes prove to you they are everything we say they are plus more . . . call us for a free trial offer and we'll ship your probe to you today. At the end of 30 days if you're not 100% satisfied, send it back and forget all about it!

Extend your trouble-shooting capability with the NEW KURZ-KASCH HI/LO PULSER!

The new HL582 Kurz-Kasch pulser (an in-circuit stimulator) puts more trouble shooting aid at your finger tips. The New HL582 is completely TTL/DTL compatible. Powered by the same source that powers the IC's being tested, the HL582 allows the operator to change the state of the node in question by pulling a low state "high" and a high state "low." All you do is touch the tip of the pulser to that point being tested, press the probe button and the node will briefly change state. Because the probe is resting in a high impedance state until activated, it will not affect the logic under test. Even if the node has several outputs and inputs connected to it, the pulser will automatically change the state. This change of state is easily detected by the Logic Probe and will not harm IC's in any way.

The combination of the HL582 Pulser and the LP520 Logic Probe allows the operator to determine if counters, registers and gates are working. If the operator selects to use the pulser in continuous mode, then the node selected has its logic changed at a 5 Hz rate. This mode of operation is ideal for testing counters and shift registers. The pulser and probe combination can detect board shorts as the pulser cannot pull up a direct hard-wired short. Board shorts, open pins, stuck gates and bad IC's can be detected without unsoldering or breaking conductors on the PC board.



WANT TO KNOW MORE ?

CALL: Telephone: 513/296-0330

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Telephone (513) 223-8161

Operating Instructions For Model LP-510, LP-520, LP-530, LP-540 SERIES LOGIC PROBES

DESCRIPTION

The Kurz-Kasch Logic Probes are designed for fast servicing and checking of integrated logic systems. With their unique multi-lamp readouts at the tips of the probes, the Logic Probes visually display the presence of correct logic levels by illumination of colored readouts marked "1" and "0". Incorrect logic levels are shown by the absence of illumination at the colored readouts.

Various optional features, described in later paragraphs, are available to significantly increase the versatility of the Logic Probes.

GENERAL SPECIFICATIONS

	Probe Series	
	LP-510 and LP-520	LP-530 and LP-540
1. Operating Power		
Vcc	4.75 to 5.5 Vdc	12 to 15 Vdc
Standby Current	25 MA	80 MA
Current For Each Readout	70 MA	50 MA
2. Nominal Logic Voltage Response		
Logic "0" Illumination (White)	0 to .8 V	0 to 1.5 V
"Gray Area" (No Illumination)	.8 to 2.4 V	1.5 to 10 V
Logic "1" Illumination (Red)	2.4 to Vcc	10V to Vcc
3. Input Impedance		
Minimum at Logic "1" Level	- Greater Than 35K ohms -	
4. Overvoltage Protection		
At Probe Tip	± 100 V. Intermittent	
5. Power Lead Reversal Protection		
Maximum Reverse Current	350 MA	0 MA

PULSE DETECTION

In the LP-520 and LP-540 series, a third readout (colored blue and marked "P") is provided in the probe tip and is illuminated for 200 milliseconds whenever a 50 nanosecond (or greater) pulse (or a pulse train) appears at the probe tip.

MEMORY/STRETCH OPTION (Probes With Suffix Letter "M")

The push-pull switch at the end of the "M" probes permits pulse detection in either "stretch" or "memory" modes. In the "stretch" mode (switch pulled out) the blue "P" indicator illuminates for 200 milliseconds in response to each single pulse (positive or negative going) of 50 nanoseconds, or greater, duration. In the "memory" mode (switch pushed in), the "P" indicator is illuminated indefinately after the first pulse or logic transition, until reset by pulling the switch out. To use the "memory" mode, first pull the switch out, then connect the probe tip to the point being examined. This initial contact will cause the "P" indicator to flash. Following the initial "P" flash, the switch should be pushed in and the probe is now ready to operate in the "memory" mode.

5-NANOSECOND PULSE CAPABILITY OPTION (Probes With Suffix Letter "S")

Probes with this option have a pulse detection capability 10 times faster than standard probes, in that a 5 nanosecond (or greater) pulse will illuminate the blue "P" indicator. Therefore, in these instructions, any 50 nanosecond limitation on pulse detection capabilities may be reduced to 5 nanoseconds for "S" probes.

3-CHANNEL INPUT OPTION (Probes With Suffix Letter "G")

Probes with the "G" option closely simulate a 3-input oscilloscope, in that two inputs are provided in addition to the probe tip input, and the blue "P" indicator will illuminate only when the probe tip and the gate input(s) are in co-incidence. When only one gate input is used, the other should be connected to Vcc or left open (implied "1") and not grounded. The shortest pulse should be connected to the probe tip input channel to insure that identical pulses will display (simulates a delay line in an oscilloscope, approximately 10 nanoseconds).

"G" OPTION PROBES ARE PROVIDED WITH THE FOLLOWING ADDITIONAL LEADS:

Black Wire - Ground - Although this lead is common with the black power lead, it should be terminated at ground points next to the signal source where measurements are being taken. This is necessary for observing pulse speeds faster than 50 nanoseconds or for verifying timing relationships. This prevents any ringing from falsly triggering the pulse detector circuit.

Green Wire - Logic Output - This is a probe output, intended to drive high impedance devices only. This lead permits oscilloscope viewing of the signal present at the probe tip. Do not terminate this lead at ground or at Vcc.

White Wires - Gate Inputs - The maximum input at either of these leads should not exceed +5.5 Vdc. The pulse detector is inhibited at an input to either lead of less than 0.8 Volts. Each input = 1 TTL load.

TO CHECK PROBE

1. Connect black power lead to ground.
2. Connect red power lead to +Vcc.
3. Touch probe tip to +Vcc, and red "1" readout should be illuminated, and blue "P" readout should momentarily (200 milliseconds) illuminate.
4. Touch probe tip to -Vcc, and white "0" readout should be illuminated, and blue "P" readout should momentarily (200 milliseconds) illuminate.

OPERATION OF THE PROBE

The red "1" readout will remain illuminated only during the time period when logic level "1" is present at the probe tip. Similarly, the white "0" readout will remain illuminated only during the time period when logic level "0" is present at the probe tip. The blue "P" readout will illuminate as the result of a transition in logic levels. Therefore, typical operating situations likely to be encountered are as follows:

1. With probe tip touching symmetrical clock source, white and red indicators will both be illuminated at one-half brilliance, and blue "P" indicator will be illuminated at full brilliance.
2. With probe tip touching positive-going high-speed pulses of short duty cycle, white "0" and blue "P" indicators will be illuminated, red "1" indicator will be illuminated on duty cycles greater than 10%. An indication of symmetry can be obtained from the relative brilliance of the "0" and "1" indicators.
3. With probe tip touching negative-going high-speed pulses of short duty cycle, red "1" and blue "P" indicators will be illuminated, white "0" indicator will

be illuminated on duty cycles greater than 10%. An indication of symmetry can be obtained from the relative brilliance of the "0" and "1" indicators.

4. Blue "P" only illuminated indicates noise in the system.

TYPICAL OPERATION OF THE GATING FEATURE (Probes With Suffix Letter "G")

In Fig. 1 at the right, "A" is the input to one of the gates. If "B" is the probe tip input, the blue "P" indicator will be illuminated. If "C" is the probe tip input, the blue "P" indicator will not be illuminated.

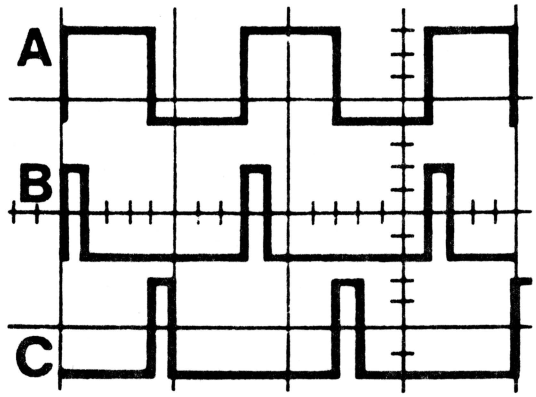


FIGURE 1

USE OF THE GATING FEATURE TO VERIFY TIMING RELATIONS (Probes With Suffix Letter "G")

Fig. 2 represents a typical digital system with square wave as a flip flop output "Q" and "$\overline{Q}$". "B" and "C" are generated each time "Q" goes positive. This relationship may be verified by connecting an input gate (white wire) to flip flop "Q" and using the probe tip at "B" or "C" as follows:

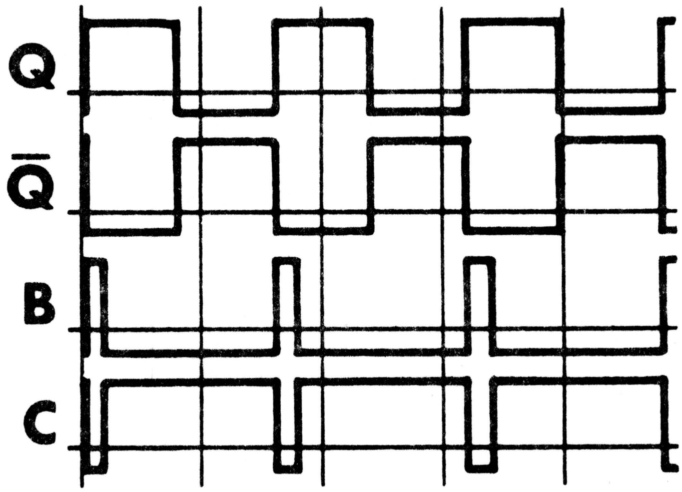


FIGURE 2

1. Connect white gate input lead to "Q" on flip flop.
2. Touch probe tip to "B" in circuit.
3. White and blue indicators will illuminate, verifying that dur- the time "Q" is positive, "B" goes from "0" to "1" and back to "0".
4. Re-connect white gate lead to "$\overline{Q}$", and repeat step #2, above.
5. Only the white indicator is illuminated, verifying that "B" is not generated during the time "$\overline{Q}$" is positive. Step #3 verified that "B" exists, but the probe pulse indicator can only be triggered when the input gates are positive.
6. By touching the probe input to "C" and connecting the gate input to "Q", the red and blue indicators will illuminate. By re-connecting the input gate to "$\overline{Q}$" only the red indicator will illuminate because no transition occurs at the probe tip when the gate is open. This may be detected by using "C" as the gate source and probing "Q".

USE OF THE GATING FEATURE IN PHASE TESTS (Probes With Suffix Letter "G")

1. Referring to Fig. 2, connect one of the input gates to "Q".
2. Touch the probe tip to "$\overline{Q}$"
3. The "0" and "1" indicators illuminate at equal intensity, but "P" indicator is unilluminated, indicating 180° out-of-phase relationship between "Q" and "$\overline{Q}$".

Kurz-Kasch, Inc.

ELECTRONICS DIVISION
2876 Culver Avenue
Dayton, Ohio 45429
Telephone 513/296-0330

END USER PRICE SCHEDULE EFFECTIVE 1/20/74

PART NUMBER	DESCRIPTION	1-9 PRICE
LP-500	TTL Logic Probe	19.95
LP-510	TTL Logic Probe	29.95
LP-520	TTL Logic Probe	69.95
LP-520-G	TTL Logic Probe (Gating Option)	79.95
LP-520-GM	TTL Logic Probe (Gating and Memory Option)	89.95
LP-520-GMS	TTL Logic Probe (Gating, Memory and Speed Option	99.95
LP-520-GS	TTL Logic Probe (Gating and Speed Option)	89.95
LP-520-M	TTL Logic Probe (Memory Option)	79.95
LP-520-MS	TTL Logic Probe (Memory and Speed Option)	89.95
LP-520-S	TTL Logic Probe (Speed Option)	79.95
LP-527	TTL Logic Probe (With BNC Connector)	79.95
LP-520-002	TTL Logic Probe (Student Proof)	79.95
LP-520-013	TTL Logic Probe (G.E. Computer)	109.95
LP-530	HTL Logic Probe	44.95
LP-540	HTL Logic Probe	69.95
LP-540-M	HTL Logic Probe (Memory Option)	79.95
LP-540-G	HTL Logic Probe (Gating Option)	79.95
LP-540-GM	HTL Logic Probe (Gating and Memory Option))	89.95
LP-540-GMS	HTL Logic Probe (Gating, Memory, and Speed Option)	99.95
LP-560	RTL Logic Probe	79.00
LP-560-M	RTL Logic Probe (Memory Option)	89.00
LP-575	C-MOS Logic Probe (Digit display)	89.00
LP-575-M	C-MOS Logic Probe (Digit display with Memory Option)	99.00
LP-575-GM	C-MOS Logic Probe (Digit display with Gating and Memory Option)	109.00
LP-576	C-MOS Logic Probe	79.00
LP-576-M	C-MOS Logic Probe (Memory Option)	89.00
LP-576-GM	C-MOS Logic Probe (Gating and Memory Option)	99.00
LG-580	TTL Square wave generator	79.95
LG-581	HTL Square wave generator	89.95
HL-582	TTL Hi Lo Pulser	89.00
IC-590	TTL, HTL IC tester battery power	169.95
IC-591	HTL, TTL IC tester AC power	295.00
IC-592	C-MOS, TTL, HTL IC tester battery battery power	—
IC-593	C-MOS, TTL, HTL IC tester AC power	—
PBB-1501	(PBB-1 Power Board Battery operated)	49.95
PBD-1502	(PBB-2 Power Board 5 volt model)	99.95
PBA-1503	(PBB-3 Power Board 0-15 volt model)	99.95
JV-1505	Junction Verifer AC Power	44.95

*All model logic probes maybe furnished with co-axial cable and BNC connector at $10.00 each.

Quantity Discounts

1-9 probes net price
10-24 probes net price less 10%
25-49 probes net price less 15%
50-99 probes net price less 20%
100-UP probes net price less 25%

ACCESSORIES

PART NUMBER	DESCRIPTION	1-9 NET
	Replacement Lamp Kit	
RB-510	colored bulbs	2.25
RB-510C	clear bulbs	2.25
RB-520	colored bulbs	3.00
RB-520-C	clear bulbs	3.00
RB-520-002	colored bulbs	3.75
RB-520-002C	clear bulbs	3.75
RB-530	colored bulbs	2.25
RB-530C	clear bulbs	2.25
RB-540	colored bulbs	3.00
RB-540C	clear bulbs	3.00
RB-560	colored bulbs	7.20
RB-560C	clear bulbs	7.20
RB-576	colored bulbs	3.00
RB-576C	clear bulbs	3.00

PROBE TIP ADAPTORS

A520-1	2¾" Long .025 Square	3.50
A520-2	3½" Long .031 x .062	3.50
A520-3	2¾" Long .025 x .040	3.50
A520-4	7¼" Long .025 x .040	3.50
A520-5	7¼" Long .025 Square	3.50
A520-6	7¼" Long .031 x .062	3.50

Note: Special adaptors available to your specifications.

PROBE TIP CONVERSION KIT COLORED WELLS WITH CLEAR BULBS

RTC-510	For LP-510 & LP-530 Series	6.25
RTC-520	For LP-520 & LP-540 Series	7.00
RF-1	Fuse, LP-520-002 (0940005)	0.90
RLG-1	"G" Probe Gating Lead Assembly	4.95
	"G" Probe Gating Connector	
RLG-2	Male	0.70
RLG-3	Female	0.70
RLC-4	Minature Coaxcable Assembly, 30", with BNC Connector	7.50

I C TESTER ACCESSORIES

IC-590-96	Cable Assembly, Remote, 18"	24.95
IC-590-97	Adapter, T.O.-5 (10 pin) to D.I.P.	7.10
IC-590-98	Adapter, T.O.-5 (8 pin) to D.I.P.	6.55
IC-590-99	Adapter, Flat Pack, to D.I.P.	11.50

Accessory Quantity Discounts

1-9 net price
10-24 net price less 10%
25-49 net price less 15%
50-99 net price less 20%
100-UP net price less 25%

Terms: Net 30 days
FOB: Dayton, Ohio

ATARI'S NEW TV
TEST PROBE - LP600 TV

This new piece of diagnostic test equipment designed in conjunction with Kurz-Kasch is the operators answer to troubleshooting his video games. The LP600 TV allows the operator to probe two (2) key test points and by reading the lighting scheme indicated by the probe, determine where the failure mode lies: (i.e. the monitor or the computer). As an example: (no video - the TV screen is black), at first look you determine the TV has power going to it because the fillament is lit in the neck of the picture tube. However, at this point you don't know whether the TV is bad or the computer is bad. So you take our your LP600 TV probe, connect it to points indicated below. If the lights in the probe illuminate the computer is good and the TV is bad. If the lights in the probe don't illuminate the computer is bad and the TV is good.

Here is how the LP600 TV works.

Almost all video games produced today has copied our sync generating circuit which is patented: (pat. no. 3793483 Nov. 24, 1972). The basic concept of digital sync generation is to produce a pulse train from a master clock and after counting these pulses you have a train with a duration of approximately 63.5 u sec; the time required for the beam of the TV to make one sweep across the screen before being reset to make the second sweep. In addition the number of sweeps are counted to equate one field so the beam can retrace the screen and start its sweeping again. Since a TV uses 525 line resolution each field utilizes 262.5 lines, whereas our displays use 261 lines per field repeatedly.

Consider now our 14.31818 MHZ clock after being divided by 2 - the result is a 7.159 MHZ signal which has been shaped into a purely digital signal. The time for one pulse to occur is $T = 1/F$ Where T = time X

1 = constant

$F = (7.159 \times 10^6)$

Therefore $X = 1/(7.159 \times 10^6)$

$X = (.13968 \times 10^{-6})$

$X = .140$ u sec

One pulse from the clock flip-flop occurs within .140 u sec. Now if you mulitply the H counter output which is, 4H + 64H + 128H = 452: (452) x (.140 x 10-6)= 63.28 u sec. the time between resets (one sweep) which creates H sync. Secondly if you multiply the V counter output which is, 1V + 4V + 256V = 261; (261) x (63.28 x 10-6) = 16,516.08 u sec. 16,516 u sec. = 16.516 m sec the time between V sync where the beam retraces the screen.

Therefore as we can see each H sync occurs every 63.28 u sec and each V sync occurs every 16.516 m sec. Now then if either counter is not counting properly the respective timing relationship will be off and the reset period will be off and the indicator lamp of the probe will not illuminate. You would then know you have a bad board instead of a bad TV.

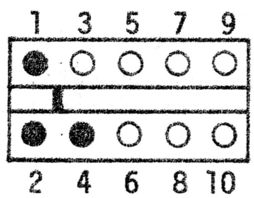
Where to connect your probe.

The first place to connect to is the +5VDC and GND of the computer board. Then decide which pattern is affiliated with your TV.

Pattern 1

(Hitachi-Zenith)

Pin 1 - Ground
Pin 2 - Video and Sync
Pin 3 - Audio



Pattern 2

(Motorola)

Pin 1 - Video and Sync
Pin 2 - Ground
Pin 4 - Audio

Whichever pattern you have, here is the procedure: (with game on)

1. Touch the tip of the probe to the appropriate terminal.

2. Interprete the lights.

EXAMPLES:

1. No video (Hitachi TV)

   A. Touch terminal - if red light indicates PCB is OK, TV is bad.

2. Scrambled sync (not TV)

   A. Touch pin - if white light does not illuminate the PCB is bad and the monitor is OK and vice-versa.

ATARI™
Innovative leisure

REBOUND

computer service manual

Bulletin 101-1

ATARI INC 14600 WINCHESTER BOULEVARD, LOS GATOS, CALIFORNIA 95030 • TELEPHONE (408) 374-2440 • TELEX 357-488

TABLE OF CONTENTS

LIST OF FIGURES AND TABLES

1. GENERAL MAINTENANCE INFORMATION

1-1. INTRODUCTION

1-2. The Atari Rebound game consists of a cabinet, TV monitor, a printed circuit board (PCB) computer, interconnecting wiring, and various cabinet-mounted circuit components. Except for a schematic, no information about the TV monitor is presented in this manual. The TV monitor is a modified Motorola XM500 unit. TV circuit malfunctions can be solved using standard TV troubleshooting techniques. However, the PCB computer requires troubleshooting techniques that may be unfamiliar to the average technician. Therefore, the troubleshooting information in this manual is dedicated to the PCB computer and its associated cabinet circuitry.

1-3. TEST EQUIPMENT

1-4. In order to test any Atari PCB, some items such as the logic probe are absolutely essential. Others are desirable and will make the test procedure easier but are not absolutely essential. Some of these instruments are available from the Atari Customer Service Department and these are: the Atari Universal Test Fixture, the Kurz-Kasch 520 Logic Probe, the Atari Video Probe and the Hewlett-Packard 10529A Logic Comparator. Other instruments that are very useful are the HP 10526T Logic Pulser and the Tektronix 465 Oscilloscope. These items are available through your local electronics supply house.

1-5. **Required Minimum Equipment:** The following items are absolutely essential to perform the test procedures presented in this manual:

a. Atari Universal Test Fixture: The Atari Universal Test Fixture can be used to test the PCB computer assemblies for Pong, Pong Doubles, Super Pong, Rebound, Space Race, Gotcha, and Quadrapong. This test fixture is equipped with a 12 inch TV monitor, two 5 volt BNC connectors for use where a regulated 5 volt source is required, and all the controls necessary to operate the PCB computers. Connector cables must be ordered separately for each different type of PCB to be tested. The test fixture and cables are available only through the Atari Customer Service Department.

b. Logic Probe: The logic probe is an instrument designed for checking the outputs of integrated circuits. The Kurz-Kasch Logic Probe, Model No. LP-520, which is available through the Atari Customer Service Department or most large electronics supply houses, is recommended. This logic probe indicates if a signal is a logic high, logic low, or changing from one state to another. Consult the operating instructions included with the probe for further details about its operation. Logic probes received from the Atari Customer Service Department are specially modified to be compatible with the 5 volt BNC connector of the Atari Universal Test Fixture.

c. Video Probe: The video probe is a very simple but extremely useful device and consists of two test clips, a length of rubber-coated, test-lead wire, and a 4.7K, 1/4 watt carbon resistor. Video probes may be obtained free from the Atari Customer Service Department or, if necessary, they can be assembled from standard components available at all electronics supply houses. To use the video probe, attach one clip to the negative (-) side of the 10 uf video coupling capacitor found near position C9 on the PCB and clip the other end to the desired signal test points as indicated in the test procedures presented in this manual. The video probe allows the desired signal to be displayed on the TV monitor screen.

1-6. **Optional Equipment:** It is possible to find 90% of the possible PCB computer malfunctions without the following items. However, if a complete set of troubleshooting equipment is desired, Atari recommends:

a. Hewlett-Packard 10529A Logic Comparator: The Hewlett-Packard 10529A Logic Comparator is used to verify correct IC operation. This device simply clips onto in-circuit ICs and instantly displays any logic state difference between the in-circuit test IC and the reference IC in the comparator. Logic differences for each pin of a 14 or 16 dual in-line package are indicated by a lamp on the comparator. If the logic comparator is purchased from the Atari Customer Service Department, it is shipped with 20 preprogrammed reference PCBs. If the device is purchased elsewhere, these PCBs must be specially programmed.

b. Hewlett-Packard 10526T Logic Pulser: The Hewlett-Packard 10526T Logic Pulser is used to stimulate in-circuit ICs so that they are driven to

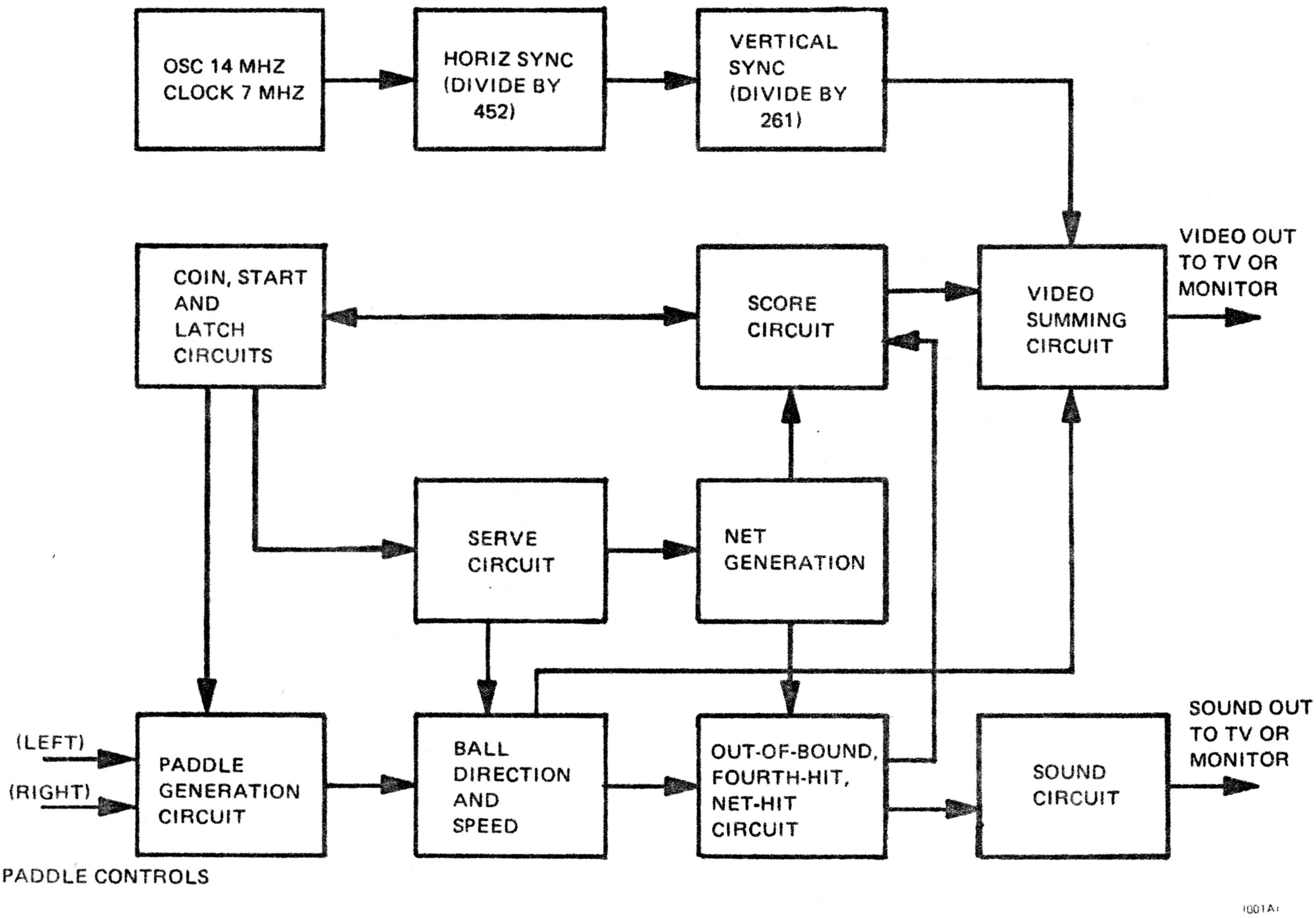


Figure 1-1. Rebound Block Diagram

their opposite states. This device is available from the Atari Customer Service Department or can be obtained from most large electronics supply houses.

c. **Tektronix 465 Oscilloscope:** The Tektronix 465 Oscilloscope is used for viewing various waveforms and should be ordered from Tektronix. Consult the manufacturer's operating instructions for details on oscilloscope operation.

1-7. GENERAL TROUBLESHOOTING APPROACH

1-8. The first step when troubleshooting malfunctions of the PCB computer is to relate the visible or audible malfunction to one or more circuits of the computer. For instance, if one of the paddle symbols is malfunctioning, study the text of the paddle circuit and then try to determine what might be causing the problem. Then, using schematics, the PCB component location diagram, and recommended test equipment, check out the paddle circuitry. Partial schematics of the computer are provided with each circuit description. Overall schematics of the computer and TV monitor, a cabinet wiring schematic, a component location diagram for the PCB computer, and a parts list are located at the rear of this manual.

1-9. BLOCK DIAGRAM DESCRIPTION

1-10. All circuitry of the computer is activated when the Rebound power cord is connected to a suitable source of ac power. Circuitry in the credit/start/electronic latch circuit automatically generates ATTRACT, $\overline{\text{ATTRACT}}$, START, and $\overline{\text{START}}$ signals. These signals are used by various cir-

cuits of the PCB computer to place the Rebound game in the attract mode.

1-11. **Attract Mode:** In the attract mode, the computer clock furnishes timing signals to various circuits of the computer. The horizontal sync and vertical sync circuits process a CLOCK signal, send timing signals to various circuits of the computer, and send horizontal sync and vertical sync signals to the TV monitor via the sync summing and video summing circuits. The paddle controls are defeated by the $\overline{\text{ATTRACT}}$ signal and the paddle circuit is forced to produce a horizontal bar across the bottom portion of the picture. Paddle data indicating what portion of the bar is being developed at any given time is continuously furnished to the ball direction and speed circuit.

1-12. The serve circuit is active during the attract mode and develops a ball symbol after the Rebound game is first energized. When the ball hits the horizontal bar at the bottom of the picture, the ball direction and speed circuit processes PADDLE DATA and BALL signals and develops HIT, $\overline{\text{HIT}}$, and motion data. The motion data is used by the horizontal and vertical ball motion circuits to develop ball velocity and direction signals. These signals are summed and furnished to various circuits of the computer. The BALL signal is also furnished to the TV monitor via the video summing circuit.

1-13. The net circuit is fully operative during the attract mode and produces a net symbol that increases in height after every second successful return of the ball across the net. However, due to the random movement of the ball during the attract mode, the ball is seldom returned more than twice before going out of bounds, hitting the net, or hitting the same point of the paddle bar four times in succession without being hit by the other paddle.

1-14. When the ball hits the net, goes out of bounds, or hits the left or right half of the paddle bar four times in succession, the out-of-bounds/fourth-hit/net-hit circuit sends a $\overline{\text{MISS}}$ signal to the sound circuit. The $\overline{\text{ATTRACT}}$ signal prevents the sound circuit from sending a SOUND OUT signal to the TV monitor when the ball hits the paddle bar or goes out of bounds, hits the net, or hits the left or right half of the paddle bar four times in succession. However, the sound circuit does send a $\overline{\text{SCORE SOUND}}$ signal to the serve circuit that causes another ball to be served.

1-15. The score circuit is partially inhibited by the START and $\overline{\text{START}}$ signals during the attract mode. Although the score of the last game is displayed on the TV screen, it is not changed when the ball goes out of bounds, hits the net, or hits the left or right half of the paddle bar four times in succession.

1-16. **Play Mode:** After a proper coin is inserted in the coin mechanism, the credit/start/electronic latch circuit lights the credit light and enables the start pushbutton. When ready, either player may press the start pushbutton, which causes the Rebound game to enter the play mode and a ball to be served.

1-17. All circuits of the game are fully operational in the play mode. An ATTRACT signal causes the paddle circuit to enable the paddle controls and generate the left and right paddle symbols. Thus, the players can move the paddles horizontally to hit the ball. Each time the paddle hits the ball, a hit sound is generated. If the ball hits the left half of the left paddle or the right half of the right paddle, the ball rebounds to the left or right, respectively, at full speed. If the ball hits the center of either paddle, the ball is caused to move straight up and down. If the ball hits the right half of the left paddle or the left half of the right paddle, the ball is caused to be moved toward the opposite side of the net symbol at a speed and trajectory that is determined by where the ball hit the paddle.

1-18. If the ball hits the net, goes out of bounds, is missed by a paddle, or hits one paddle four times in succession, the score display is appropriately changed by the score circuit, a miss sound is generated, and another ball is served. Each time the ball is returned two times, the net is slightly increased in height. The net can be incremented ten times but is reduced to its minimum level each time the ball goes out of bounds, hits the net, is missed, or hits the same paddle four successive times. The game continues until one player accrues a score of 11 or 15, depending on how the game is programmed. At this point, the game reverts to the attract mode. If the game has been programmed for two plays per coin, a second game may be started by pressing the start pushbutton.

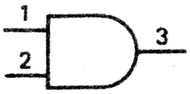
1-19. LOGIC SYMBOLOGY

1-20. Table 1-1 describes the operation of the most common logic circuits found on the computer board. Those not covered in the table are explained at their first appearance in the computer board circuit description in Section 2. Logic circuits are identified in the text and on the schematic by their actual grid location on the PCB and their output pin number, e.g., gate A6-3 would be the gate with output pin 3 in the logic package at location A6 on the PCB. The logic levels on the PCB are 0 to +0.4 volts for LO and +2.6 to +5 volts for HI. Signal names overscored (e.g., $\overline{\text{START}}$ and pronounced "start not") go LO to initiate events and those not overscored go HI when active. Overscored signals are always at the logic level opposite to that of their non-overscored counterparts, i.e., $\overline{\text{START}}$ is always at a logic level opposite to START.

Table 1-1. Logic Symbology

<table>
<tr><th>SYMBOL</th><th>TRUTH TABLE/TIMING</th><th>OPERATION</th></tr>
<tr><td>

AND GATE



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<table>
<tr><th>1</th><th>2</th><th>3</th></tr>
<tr><td>LO</td><td>LO</td><td>LO</td></tr>
<tr><td>LO</td><td>HI</td><td>LO</td></tr>
<tr><td>HI</td><td>LO</td><td>LO</td></tr>
<tr><td>HI</td><td>HI</td><td>HI</td></tr>
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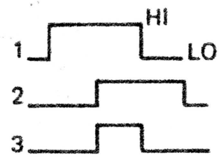

</td><td>Output is HI only when <u>all</u> inputs are HI, otherwise output is LO. Rule applies for any number of inputs.</td></tr>
<tr><td>

OR GATE

</td><td>

<table>
<tr><th>1</th><th>2</th><th>3</th></tr>
<tr><td>LO</td><td>LO</td><td>LO</td></tr>
<tr><td>LO</td><td>HI</td><td>HI</td></tr>
<tr><td>HI</td><td>LO</td><td>HI</td></tr>
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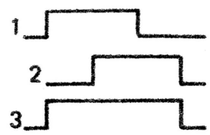

</td><td>Output is HI when any input is HI. Output is LO only when <u>all</u> inputs are LO.</td></tr>
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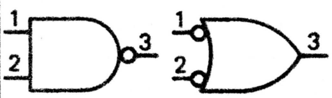
NAND GATE



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<table>
<tr><th>1</th><th>2</th><th>3</th></tr>
<tr><td>LO</td><td>LO</td><td>HI</td></tr>
<tr><td>LO</td><td>HI</td><td>HI</td></tr>
<tr><td>HI</td><td>LO</td><td>HI</td></tr>
<tr><td>HI</td><td>HI</td><td>LO</td></tr>
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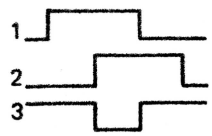
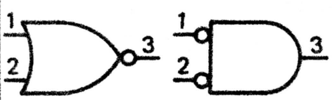


</td><td>Output is LO only when <u>all</u> inputs are HI, otherwise output is HI.</td></tr>
<tr><td>

NOR GATE



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<tr><td>LO</td><td>LO</td><td>HI</td></tr>
<tr><td>LO</td><td>HI</td><td>LO</td></tr>
<tr><td>HI</td><td>LO</td><td>LO</td></tr>
<tr><td>HI</td><td>HI</td><td>LO</td></tr>
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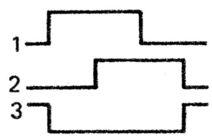
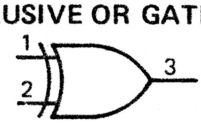


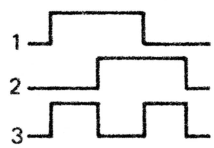
</td><td>Output is LO when any input is HI. Output is HI only when <u>all</u> inputs are LO.</td></tr>
<tr><td>

EXCLUSIVE OR GATE



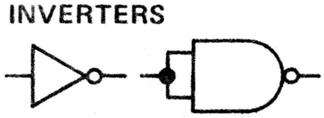
</td><td>

<table>
<tr><th>1</th><th>2</th><th>3</th></tr>
<tr><td>LO</td><td>LO</td><td>LO</td></tr>
<tr><td>LO</td><td>HI</td><td>HI</td></tr>
<tr><td>HI</td><td>LO</td><td>HI</td></tr>
<tr><td>HI</td><td>HI</td><td>LO</td></tr>
</table>



</td><td>Output is HI when <u>either but not both</u> inputs are HI, otherwise output is LO.</td></tr>
<tr><td>

INVERTERS



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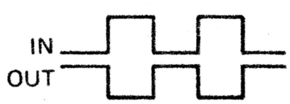
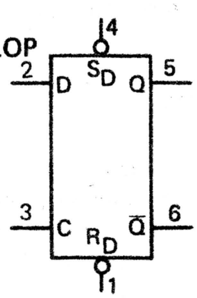


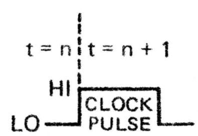
</td><td>The 2-input NAND or NOR gate can be used as inverters by tying one input to a fixed level or tying both inputs together.</td></tr>
<tr><td>

D-TYPE FLIP-FLOP



</td><td>

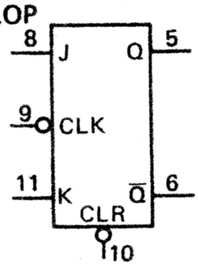
<table>
<tr><th colspan="2">t = n</th><th>t = n + 1</th></tr>
<tr><th>D</th><th>Q</th><th>Q</th></tr>
<tr><td>LO</td><td>LO</td><td>LO</td></tr>
<tr><td>LO</td><td>HI</td><td>LO</td></tr>
<tr><td>HI</td><td>LO</td><td>HI</td></tr>
<tr><td>HI</td><td>HI</td><td>HI</td></tr>
</table>



Truth Table valid only when S_D and R_D are both HI

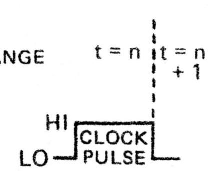
</td><td>When both S_D (direct set) and R_D (direct reset) are HI, level at input D is transferred to output Q when input C (clock) goes HI. A LO on S_D forces $\overline{Q}$ HI and Q LO. A LO on R_D forces $\overline{Q}$ HI and Q LO. S_D and R_D predominate over all other inputs.</td></tr>
<tr><td>

J-K MASTER SLAVE FLIP-FLOP



</td><td>

<table>
<tr><th colspan="3">t = n</th><th colspan="2">t = n + 1</th></tr>
<tr><th>J</th><th>K</th><th>Q</th><th>Q</th><th>$\overline{Q}$</th></tr>
<tr><td>LO</td><td>LO</td><td>–</td><td colspan="2">NO CHANGE</td></tr>
<tr><td>LO</td><td>HI</td><td>–</td><td>LO</td><td>HI</td></tr>
<tr><td>HI</td><td>LO</td><td>–</td><td>HI</td><td>LO</td></tr>
<tr><td>HI</td><td>HI</td><td>LO</td><td>HI</td><td>LO</td></tr>
<tr><td>HI</td><td>HI</td><td>HI</td><td>LO</td><td>HI</td></tr>
</table>



Truth Table valid only when CLR is HI

</td><td>When CLR is HI and:

1. J and K are both LO, clock pulse has no effect on outputs Q and $\overline{Q}$.
2. J and K are at opposite logic levels, negative-going clock edge transfers J level to Q and K level to $\overline{Q}$.
3. J and K are both HI, each negative-going clock edge alternates outputs Q and $\overline{Q}$.
4. LO on CLR forces and holds Q LO and $\overline{Q}$ HI.

</td></tr>
</table>

(U02A)

2. CIRCUIT DESCRIPTION

2-1. POWER SUPPLY

2-2. The power supply circuitry for the Rebound computer is shown in Figure 2-1. Input single-phase, 60 Hz, 115 vac power is routed through the front and rear interlocks, an ac line filter, and a 1A fuse to the primary of transformer T1. This transformer steps the input voltage down to 16.5 vac (under load), which is then applied to the rectifying, filtering, and regulating circuits of the computer.

2-3. The 16.5 vac output of T1 is full-wave rectified by diodes CR1 and CR2, and the pulsating dc output of these diodes is filtered by capacitor C28. A voltage regulator composed of integrated circuit LM309 or LM309K and resistor R4 receives the filtered dc voltage and provides a highly regulated +5 vdc output to the circuits of the computer. Resistor R4 increases the current capacity of the power supply. Capacitors C1 and C6 through C14 provide filtering for the +5 vdc bus.

2-4. COMPUTER CLOCK

2-5. Figure 2-2 shows the circuitry of the computer clock. Inverting amplifiers F9-12 and F9-2, resistors R5 and R6, capacitors C4 and C5, and crystal X1 form the oscillator portion of the clock circuit. Crystal X1 is in the feedback circuit of the oscillator and functions as a 14.3181 MHz narrow-band filter. Thus, the oscillator circuit is forced to oscillate at a frequency of 14.3181 MHz. The 14.3181 MHz signal taken from the output of amplifier F9-12 is routed through inverter F9-10 to the input of flip-flop J4-5/6. This flip-flop divides the input signal by 2 and delivers 7.159 MHz CLOCK and $\overline{\text{CLOCK}}$ signals to the logic circuits of the computer.

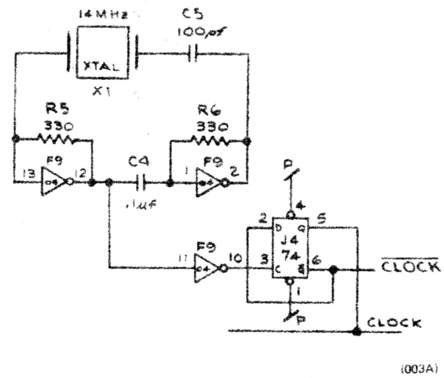


Figure 2-2. Computer Clock

2-6. HORIZONTAL SYNC CIRCUITRY

2-7. Horizontal sync for the TV monitor and timing signals for various circuits of the computer are supplied by the circuitry shown in Figure 2-3. This circuitry is composed of a counter circuit (H5, F5, and H4); NAND gates F4-6, K4-3, and K4-11; AND gate F7-3; inverter D4-4; and flip-flops J4-9/8, K5-5/6, and K5-9/8. The counter receives the 7.159 MHz CLOCK signal from the computer clock and produces numerous submultiples of the CLOCK signal that are designated 1H, 2H, 4H, 8H, 16H, 32H, 64H, 128H, 256H, and $\overline{\text{256H}}$. These submultiples are distributed to various logic circuits of the computer for timing and signal development purposes. The development of the H SYNC, $\overline{\text{H SYNC}}$, H BLANK, $\overline{\text{H BLANK}}$, H RESET, and $\overline{\text{H RESET}}$ signals is discussed in the following paragraphs. Development and timing of other signals related to the submultiples of the CLOCK signal are discussed in other portions of this manual.

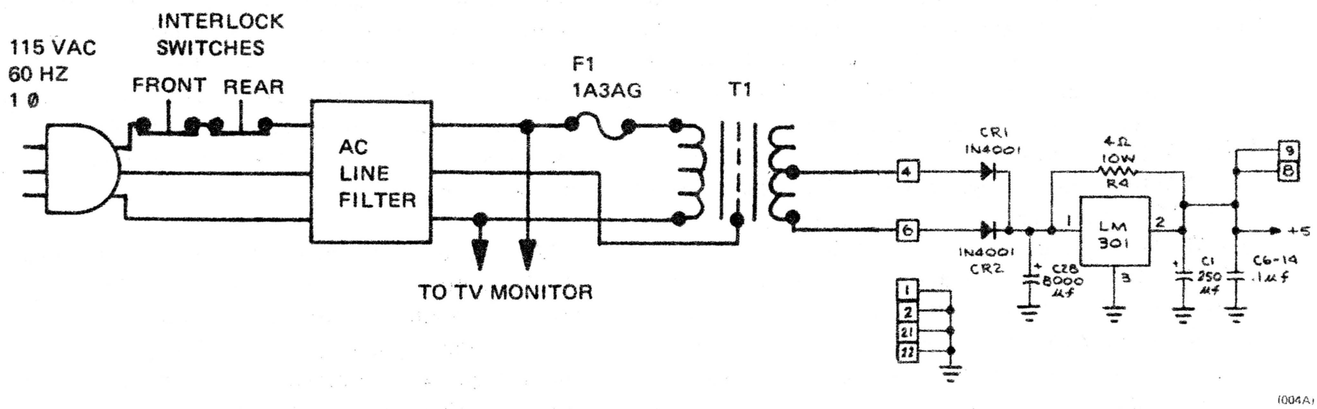


Figure 2-1. Power Supply

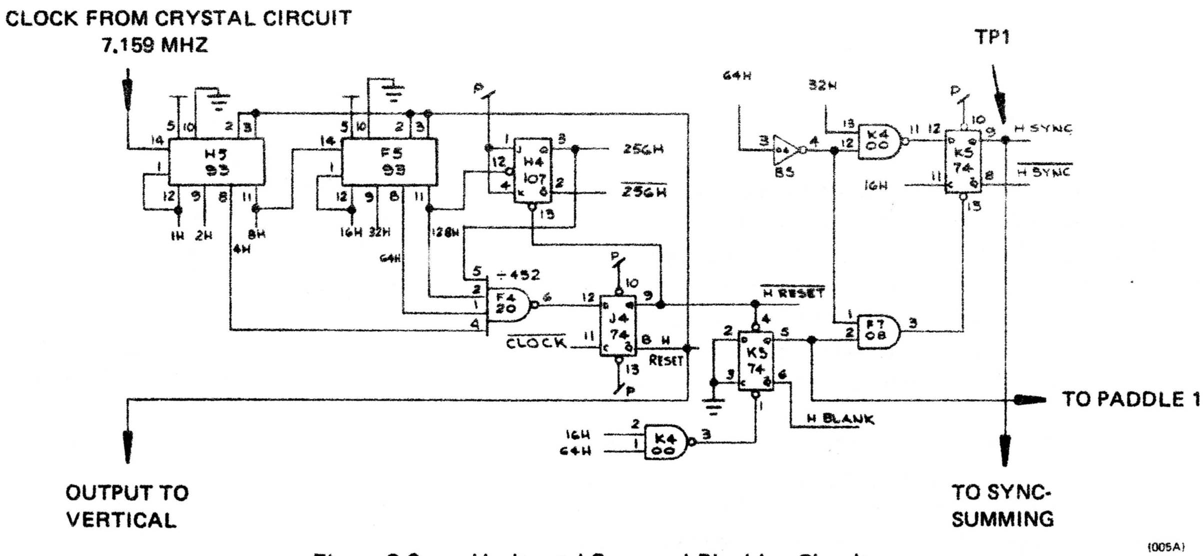


Figure 2-3. Horizontal Sync and Blanking Circuitry

2-8. Each TV line of the Rebound game is approximately 63 usec long, which is equivalent to the time it takes the counter to count 453 CLOCK pulses after being reset. At the count of 452, the 256H, 128H, and 4H signals are all high. As a result, the output of NAND gate F4-6 goes low. When the next $\overline{\text{CLOCK}}$ pulse occurs, the Q output of flip-flop J4-9/8 goes low and the $\overline{\text{Q}}$ output goes high. The Q output is used to reset flip-flop H4-3/2 of the counter, to set flip-flop K5-5/6, and for other signal development purposes on the computer. The $\overline{\text{Q}}$ output of J4-9/8 is used to reset counters H5 and F5 and is also sent to the vertical sync circuitry.

2-9. Setting flip-flop K5-5/6 causes the $\overline{\text{Q}}$ output to go low, which establishes the leading edge of the $\overline{\text{H BLANK}}$ pulse, and the Q output to go high, which establishes the leading edge of the H BLANK pulse. The H BLANK pulse is sent to the paddle logic and to AND gate F7-3. Before the count 64H is reached, the output of inverter B5-4 is high. Therefore, the output of AND gate F7-3 is high. Signals 16H and 32H are both high at the count of 48. Consequently, the output of NAND gate K4-11 goes low, and the clock input (pin 11) of flip-flop K5-9/8 is enabled. With a low applied to pin K5-12 and highs applied to pins K5-10, K5-11, and K5-13 of flip-flop K5-9/8, the Q output of the flip-flop goes low, which forms the leading edge of the H SYNC pulse, and the $\overline{\text{Q}}$ output goes high, which forms the leading edge of the $\overline{\text{H SYNC}}$ pulse. At the count of 64, the 64H signal goes high, causing flip-flop K5-9/8 to change states and form the trailing edge of the H SYNC and $\overline{\text{H SYNC}}$ pulses. At the count of 80, the 16H and 64H signals are high, causing a low to be applied to the clear input (pin 1) of flip-flop K5-5/6. As a result, the flip-flop changes state and thereby forms the trailing edges of the H BLANK and $\overline{\text{H BLANK}}$ signals. The $\overline{\text{H SYNC}}$ and $\overline{\text{H BLANK}}$ are both used by other circuits of the computer, and the H SYNC signal is used by circuits of the computer and is sent to the TV monitor via the sync summing and video summing circuits.

2-10. VERTICAL SYNC CIRCUITRY

2-11. Vertical sync for the TV monitor and signal development and timing signals for various circuits of the computer are supplied by the vertical sync circuitry, which is shown in Figure 2-4. The vertical sync circuitry is composed of a counter circuit (J3, H3, and H4), NAND gates H2-12 and H2-6, and flip-flops J2-9/8 and H1-3/11. During operation, the counter receives the H RESET signal from the horizontal sync circuitry and produces numerous submultiples of the H RESET signal that are designated 1V, 2V, 4V, 8V, 16V, 32V, 64V, 128V, 256V, and $\overline{\text{256V}}$. These submultiples are distributed to various logic circuits of the computer for timing and signal development purposes. The development of the $\overline{\text{V RESET}}$, V RESET, and $\overline{\text{V SYNC}}$ signals is discussed in the following paragraphs. Development and timing of other signals related to the submultiples of the H RESET signal are discussed in other portions of the manual.

2-12. It requires 1/60.08 second to develop one field of the TV picture for the Rebound game, which is the time it takes the counter to count 262 H RESET pulses after being reset. At the count of 261, the 256V, 4V, and 1V signals are all high. As a result, the output of NAND gate H2-12 goes low. When the next H RESET pulse occurs, the Q output ($\overline{\text{V RESET}}$) of flip-flop J2-9/8 goes low and the $\overline{\text{Q}}$ out-

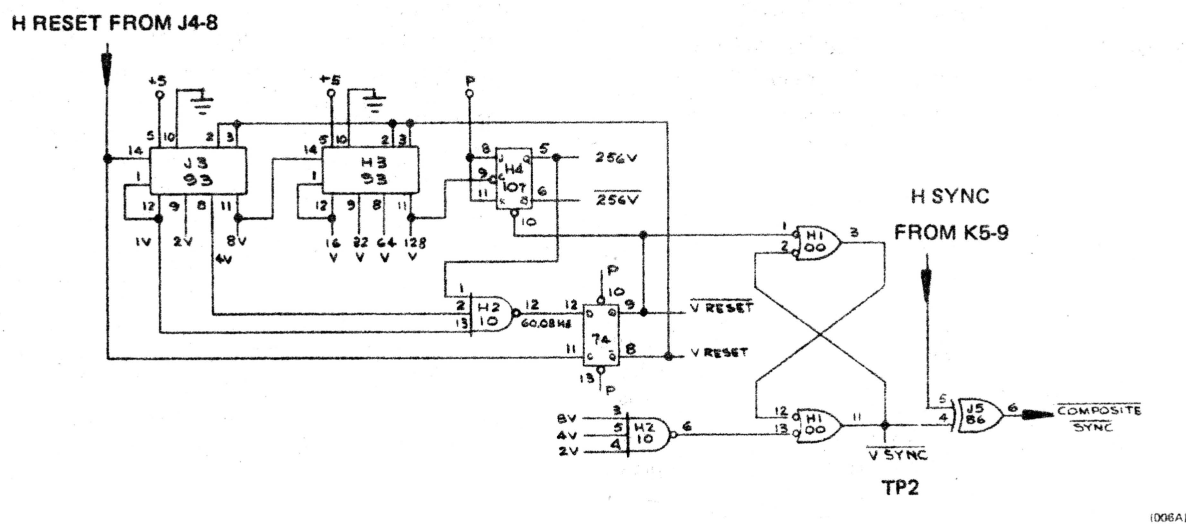


Figure 2-4. Vertical Sync and Sync Summing Circuitry

put (V RESET) goes high. The Q output is used to reset flip-flop H4 of the counter, to set flip-flop H1-3/11, and for other timing and signal development purposes on the computer. The $\overline{Q}$ output is used to reset counters J3 and H3 and is also used for other timing and signal development purposes on the computer.

2-13. Setting flip-flop H1-3/11 causes the output at pin H1-11 to go low, which forms the leading edge of the $\overline{\text{V SYNC}}$ pulse. Fourteen H RESET pulses later, signals 8V, 4V, and 2V are all high. Consequently, the output of NAND gate H2-6 goes low, which resets flip-flop H1-3/11. Resetting flip-flop H1-3/11 forms the trailing edge of the $\overline{\text{V SYNC}}$ pulse, which is sent to sync summing gate J5-6 and to other circuits of the computer for signal timing and developmental purposes.

2-14. SYNC SUMMING

2-15. Exclusive OR gate J5-6 (shown in Figure 2-4) is used for sync summing. H SYNC pulses are applied to pin 5 of this gate, and $\overline{\text{V SYNC}}$ pulses are applied to pin 4. The logic of the exclusive OR gate causes the $\overline{\text{V SYNC}}$ pulse to be serrated by the H SYNC pulses. Serrating the $\overline{\text{V SYNC}}$ pulse keeps the horizontal oscillator of the TV monitor synchronized during vertical retrace. The output of the exclusive OR gate is sent to the video summing circuit and consists of a serrated vertical sync pulse (containing 14 serrations) followed by 248 horizontal sync pulses. Therefore, one field of the TV picture consists of 248 viewable lines. Since no interlace provisions are incorporated into the circuitry of the computer, successive fields are laid approximately on top of one another, resulting in a picture frame that contains approximately 248 lines. This frame is repeated 30.04 times per second.

2-16. ELECTRONIC LATCH CIRCUIT

2-17. The electronic latch circuit is shown in Figure 2-5 and consists of transistors Q1, Q2, and Q3 and associated circuitry, inverter E9-4, and an antenna. The antenna is mounted within the Rebound cabinet; all other components of the electronic latch circuit are mounted on the computer board. The latch circuit has four functions, which are described in the following paragraphs.

2-18. The first function of the latch circuit is to initialize (Q high) flip-flop D8-9/8 of the one/two-play circuit and flip-flop E8-5/6 of the start circuit when power is first turned on. This function results from the fact that the latch circuit stabilizes with the collector of transistor Q3 at a high state after power is turned on. This high is inverted by E9-4 and used to preset the Q outputs of flip-flops D8-9/8 and E8-5/6 to a high level. Presetting these two flip-flops disables the start circuitry and places the Rebound game in the attract mode, which is discussed in another section of this manual.

2-19. The second function of the latch circuit is to furnish enabling levels to the preset inputs of flip-flops D8-9/8 and E8-5/6 when the credit circuit has determined that a proper coin has been deposited. As described in the text of the credit circuitry, flip-flop E8-8 produces a negative-going pulse when a proper coin is deposited. This pulse is routed through diode CR8 and resistor R14 to the base of transistor Q2, turning on the transistor. Providing transistor Q1 is

not turned on by the antenna circuit (discussed in the next paragraph), the high developed at the collector of Q2 turns on transistor Q3. Turning on Q3 latches transistors Q2 and Q3 in the on state, which perpetuates the high levels applied to the preset inputs of flip-flops D8-9/8 and E8-5/6.

2-20. The credit and start circuitry is sensitive to any accidental or player-produced static charges. If not offset, these charges can enable the start circuitry. To offset static charges, a static suppression circuit is incorporated into the circuitry of the Rebound game. This circuit consists of an antenna within the Rebound cabinet, and diode CR7 and transistor Q1 on the computer board. When static charges are sensed by the antenna, a positive level is impressed at the base of transistor Q1, turning on Q1. Turning on Q1 turns off transistor Q3, which causes the start circuit to be inhibited and the attract mode to be enabled as previously described.

2-21. The fourth function of the electronic latch circuit is to furnish a low preset level to flip-flops D8-9/8 and E8-5/6 at the end of one or two games, as determined by the two-play/one-play circuit. When the two-play/one-play circuit senses that game credit has expired, the output of NAND gate D7-3 is forced low. This low is routed through diode CR6 to the base of transistor Q3, turning it off. Turning off Q3 unlatches the electronic latch circuit, causing a low to be furnished to flip-flops D8-9/8 and E8-5/6 via inverter E9-4. This low is used to place the Rebound game in the attract mode and inhibit the start circuitry.

2-22. CREDIT CIRCUIT

2-23. The credit circuit is shown in Figure 2-5. This circuit consists of the coin deposit mechanism; diodes CR3 and CR4; capacitors C17, C18, C19, and C20; resistors R7, R12, and R13; timer D9; inverters E9-8 and E9-6; flip-flops E9-10/12, E8-8, D8-5, and D8-9/8; NAND gate D7-3; NOR gate C8-1; a light emitting diode (LED); and the 2P/1P switch. Except for the LED and coin mechanism, all of the foregoing components are located on the computer board. The LED (credit light) and coin mechanism are located on the front panels of the Rebound cabinet.

2-24. During the time a proper coin is being deposited, a microswitch in the coin deposit mechanism is actuated. Actuating the microswitch produces a negative-going pulse that is applied to a coil of a coin counter and, via diode CR3, to pin 13 of flip-flop E9-10/12, setting the flip-flop. This flip-flop is used to prevent transients produced by bouncing contacts of the microswitch from disturbing the circuits of the computer. The low produced at pin 10 of this flip-flop inhibits part of the start circuit and triggers timer D9. At the same time, the high output at pin 12 of the flip-flop is applied to pin 2 of NOR gate C8-1 and to pins 12 and 13 of flip-flop E8-8. The timer delays the pulse from flip-flop E9-10/12 by 10 milliseconds and then applies it, via inverter E9-8, to flip-flop E8-8, triggering it. Delaying the triggering of flip-flop E8-8 by 10 milliseconds prevents the accidental or player-induced vibrations that might actuate the coin microswitch from triggering flip-flop E8-8 and eventually enabling the Rebound game.

2-25. The negative-going output of flip-flop E8-8 is sent to the electronic latch circuit and is also applied to the clear inputs of flip-flops D8-5 and D8-9/8. The resulting high from the electronic latch circuit and the low from flip-flop E8-8 cause the Q output of flip-flop D8-9/8 to go low. Flip-flop D8-5 is part of a two-play/one-play circuit and is discussed further in subsequent text. The low output of flip-flop D8-9/8 furnishes one enabling input to NOR gate C8-1 and disables NAND gate D7-3. An enabling high level for the start circuitry is taken from the $\overline{Q}$ output of flip-flop D8-9/8. This $\overline{Q}$ output is also inverted and used to forward bias the LED of the front panel credit indicator, which informs the game player that his coin has been accepted and he may start the game when ready.

2-26. After the coin has passed the microswitch, the switch returns to its normally closed position, which resets flip-flop E9-10/12. Resetting this flip-flop clears flip-flop E8-8, sends a high enabling level to the start circuitry, and enables NOR gate C8-1. Enabling NOR gate C8-1 causes another high enabling level to be sent to the start circuitry. Diode CR4 damps the inductive transient produced when the ground is removed from the coil of the coin counter. In addition, diode CR3 protects integrated circuit E9 from the positive-going inductive transients from the coin counter coil.

2-27. The two-play/one-play circuit is part of the credit circuit and consists of flip-flops D8-5 and D8-9/8, NAND gate D7-3, and the 2P/1P switch. This circuit allows the Rebound game to be set up to provide one game or two games for each coin accepted by the credit circuitry.

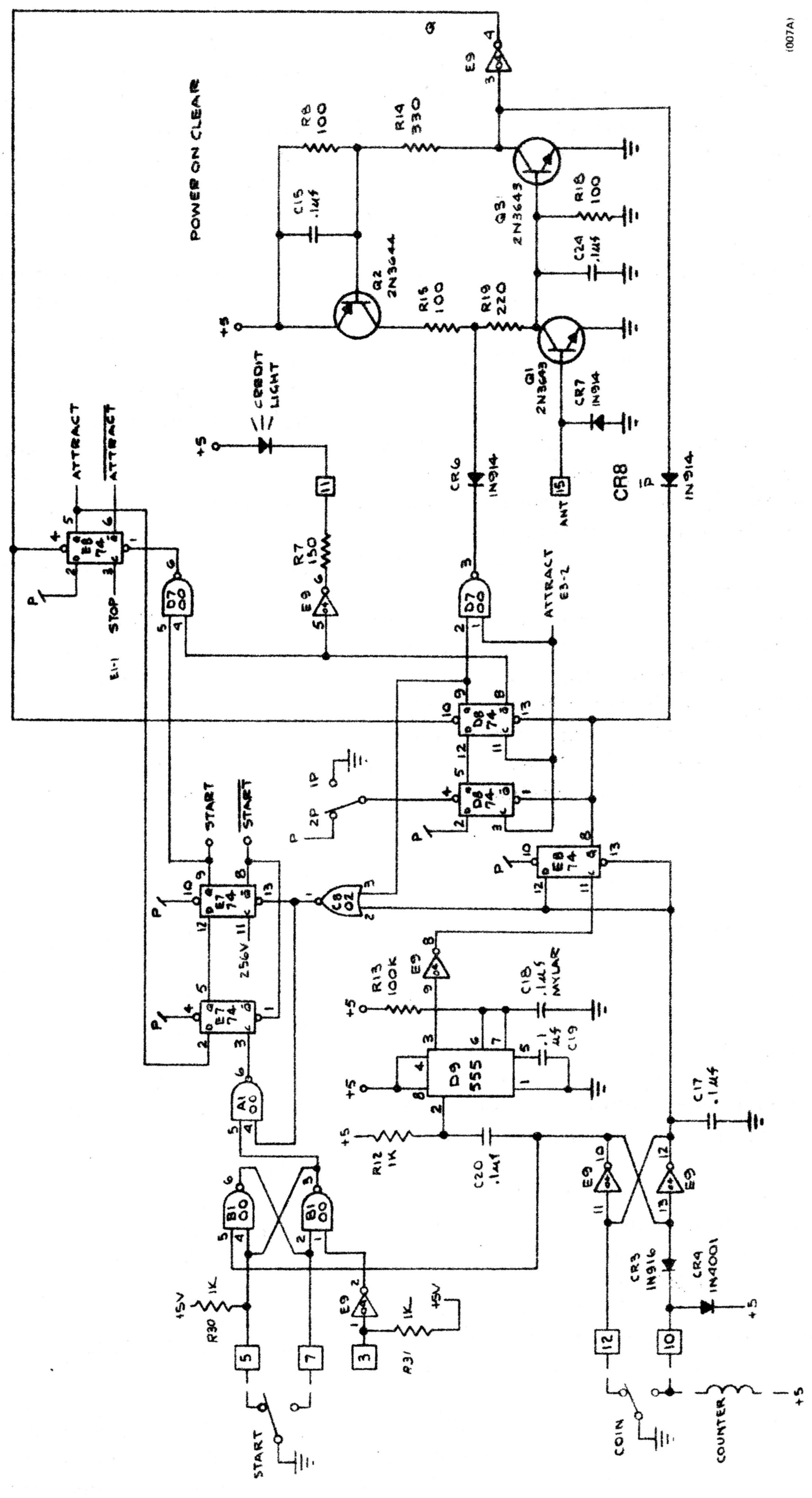


Figure 2-5. Credit, Start, and Electronic Latch Circuitry

2-28. For example, if the 2P/1P switch is set to 1P, a high is produced at the Q output of flip-flop D8-5. Therefore, when the game is over and the ATTRACT signal from flip-flop E8-5/6 goes high, the high output of flip-flop D8-5 is clocked to the Q output of flip-flop D8-9/8. This high Q output forces the output of NOR gate C8-1 to go low, which inhibits the start circuitry. In addition, the high Q output in combination with the high ATTRACT signal forces the output of NAND gate D7-3 low, which unlatches the electronic latch circuitry as described in the electronic latch text. The low $\overline{\text{Q}}$ output of flip-flop D8-9/8 turns off the credit light and also inhibits the start circuitry via NAND gate D7-6.

2-29. If the 2P/1P switch is set to 2P, a low is produced at the Q output of flip-flop D8-5 when the negative-going pulse from flip-flop E8-8 occurs. Consequently, when the game is over, the fixed high at the D input of flip-flop D8-5 is clocked to the Q output of this flip-flop, but no change occurs at the Q output of flip-flop D8-9/8. Therefore, the outputs of NOR gate C8-1 and NAND gate D7-3 remain high, allowing the start circuitry to remain enabled. When ready, the game player may press the start pushbutton to begin the second game. At the end of the second game, the high output of flip-flop D8-5 is clocked to the Q output of flip-flop D8-9/8 by the high ATTRACT signal. This high Q output, in combination with the low $\overline{\text{Q}}$ output and the high ATTRACT signal, inhibits the start circuitry as previously described.

2-30. START CIRCUIT

2-31. The start circuit is shown in Figure 2-5 and consists of inverter E9-2; flip-flops B1-6/3, E7-5, E7-9/8, E8-5/6; AND gate A1-6; NAND gate D7-6; and the start switch. The start pushbutton switch is located on the front panel of the Rebound game; all other components of the start circuit are located on the computer board.

2-32. Once the credit light is lit, the Rebound game is started by pressing the start pushbutton. Pressing and releasing the pushbutton sets and resets flip-flop B1-6/3, causing a positive-going pulse to be applied to pin 5 of NAND gate A1-6. Pin 4 of NAND gate A1-6 is high whenever game credit has been established by the credit circuit. Consequently, the high ATTRACT signal present at pin 2 of flip-flop E7-5 is clocked by the positive-going trailing edge of the pulse produced at the output of NAND gate A1-6, causing the Q output of flip-flop E7-5 to go high. When the start pushbutton is released, flip-flop B1-6/3 is reset. This flip-flop is used to prevent transients that are produced by the contacts of the start pushbutton from disturbing the circuits of the computer.

2-33. Just before vertical sync, the 256V signal clocks the high output of flip-flop E7-5 through to the Q output of flip-flop E7-9/8. This high output is the START signal, which is applied to NAND gate D7-6 and various other circuits of the computer. The $\overline{\text{START}}$ signal is used to clear flip-flop E7-5 and is also used by other circuits of the computer to start the Rebound game.

2-34. Pin 4 of NAND gate D7-6 is high whenever game credit has been established by the credit circuit. As a result, the high output of flip-flop E7-9/8 forces the output of NAND gate D7-6 low. This low causes flip-flop E8-5/6 to change states, resulting in a low ATTRACT signal and a high $\overline{\text{ATTRACT}}$ signal. The $\overline{\text{ATTRACT}}$ signal is sent to various circuits of the computer, and the ATTRACT signal is sent to flip-flops D8-5 and D8-9/8, to NAND gate D7-3, and to various other circuits of the computer. These attract signals cancel the attract mode and permit the play mode to proceed. When the game is over, a high STOP signal clocks the fixed high level at pin 2 of flip-flop E8-5/6 through to the Q output (ATTRACT signal). The ATTRACT signal is sent to the two-play/one-play circuit and to various other circuits of the computer. The two-play/one-play circuit is discussed in the text pertaining to the credit circuitry.

2-35. WINDOWS

2-36. The term window is one that has been coined to explain the process of gating the TV lines so that they can only appear within certain limits. The most confusing thing about the window concept is that it takes information from the vertical sync circuit to produce a horizontal window and vice versa. For example, Figure 2-6 correlates the vertical signals required to produce a horizontal window between vertical positions 64V and 128V with the window produced on the TV screen. Thus, if the 64V and $\overline{\text{128V}}$ signals from the vertical sync circuits are ANDed, a signal develops that can be used to blank the electron beam of the picture for all TV lines except those occurring between vertical positions 64V and 128V. As a result, a bright band between positions 64V and 128V appears on the screen of the picture tube. The remainder of the screen remains dark.

2-37. SCORE CIRCUIT

2-38. Figure 2-7 shows the circuitry of the score circuit. This circuitry consists of the score window circuitry, left and right score counter circuits, multiplexers, a BCD-to-seven segment decoder, a score segment window circuit, and a stop circuit. Each of these circuits is discussed in the following text.

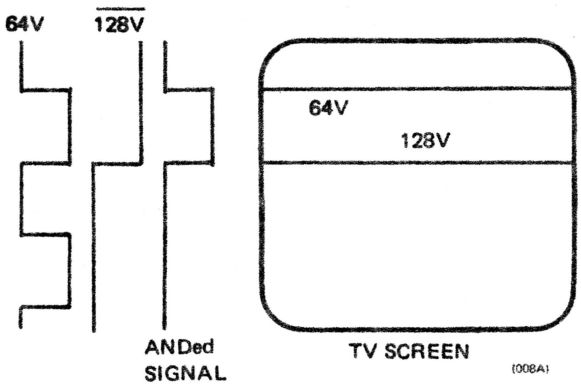


Figure 2-6. Development of a Typical Horizontal Window

2-39. Score Window Circuitry: The score window circuitry consists of NOR gate C8-13, AND gate F7-11, exclusive OR gates J5-8 and J5-11, NAND gates J6-3 and J6-6, negative-true AND gate K6-4, and inverter D4-6. Horizontal timing signals $\overline{256H}$, 64H, 256H, and 128H and vertical timing signals 64V, 32V, and 128V are matrixed to define the two score display areas. The left score display area begins at horizontal position 128H and ends at 192H, and the right score display area begins at horizontal position 320H and ends at 394H. Both score windows are located between vertical positions 32V and 64V. When the electron beam of the picture tube is within either of the two score display areas, the output of gate K6-4 is high. This high level is used to enable BCD-to-seven segment decoder/driver K7, which is discussed in subsequent text.

2-40. Score Counter Circuits: The left score counter circuit consists of decade counter K9 and J-K flip-flop H9-5/6, and the right score counter circuit consists of decade counter J9 and J-K flip-flop H9-3/2. These two counters are identical, therefore, only the left counter is described in the following text.

2-41. Decade counter K9 is reset to zero at the beginning of the game when the START signal goes high. At the same time, the Q output of flip-flop H9-5/6 is cleared to a low state and the $\overline{Q}$ output is cleared to a high state by a low $\overline{START}$ signal. During the game, high level inputs from the out-of-bounds/fourth-hit/miss circuitry for the right player are accumulated by the left score counter. The accumulated score is read out of K9 at pins 1, 9, 8, and 11 in BCD format. BCD output 1 from pin 1 is sent to the ball direction and speed circuitry, to NAND gate F8-6 of the stop circuit, and to multiplexer K8, BCD output 2 from pin 9 is sent to multiplexer K9, and BCD output 4 from pin 8 is sent to multiplexer J8 and the 11/15 score switch of the stop circuit. BCD output 8 from pin 11 is sent to J-K flip-flop H9-5/6 and multiplexer J8. Each time the BCD count changes from 1001 (decimal 9) to 0000 (decimal 10), flip-flop H9-5/6 is toggled, causing the Q output to go low. This low output of flip-flop H9-5/6 is used along with a fixed high input to pin 6 of multiplexer K8 to form BCD 0001, which is used to cause a 1 to appear in the tens position of the score. During the time the score is nine or less, the $\overline{Q}$ output of flip-flop H9-5/6 is high. This high output is used with the fixed high input to pin 6 of multiplexer K8 to form BCD 1111, which is used to cause no number to be generated for the tens position of the score.

2-42. Multiplexers and BCD-to-Seven Segment Decoder/Driver: The BCD score inputs to multiplexers K8 and J8 are sequentially gated to a BCD-to-seven segment decoder/driver by the 32H and 64H signals from the horizontal sync circuit. These gating signals are sequenced such that the tens information for the left score is gated first and is followed by the units information for the left score, the tens information for the right score, and finally the units information for the right score. When allowed by a high SCORE WINDOW signal, decoder/driver K7 sends a seven-bit code (signals a through g) to a score segment window circuit.

2-43. Score Segment Window Circuit: The score segment window circuit consists of NAND gates J7-12, J7-8, H7-6, J7-6, F8-8, H7-12, H7-8, J6-11, and F6-12; NOR gate K6-1 used as an inverter; negative-true AND gates H6-6, K6-13, and H6-12; negative-true OR gate H8-8; and inverters F9-4 and F9-8. Timing signals 4H, 8H, 4V, 8V, 16H, and 16V from the horizontal sync and vertical sync circuits are logically processed and used to enable the appropriate combination of NAND gates J7-12, J7-8, H7-6, J7-6, F8-8, H7-12, and H7-8 to allow various combinations of score segment signals (a through g) to reach negative-true OR gate H8-8. These sequenced score segment signals are ORed along with a $\overline{NET}$ signal from the net circuit to form the SCORE signal which is sent to the video summing circuit.

2-44. Stop Circuit: NAND gates F8-6 and F8-12 and negative-true OR gate J6-8 form a stop circuit. NAND gate F8-6 receives tens information from flip-flop H9-5/6 and units information from counter K9. When the 11/15 score switch is open, NAND gate F8-6 is enabled when the left score reaches 11. Alternately, when the 11/15 score switch is closed, NAND gate F8-6 is enabled when the left score reaches 15. NAND gate F8-12 receives inputs from the right score counter circuitry and operates exactly like NAND gate F8-6. When the output of either NAND gate goes low, it signifies that one player has accumulated a score of 11 or 15. This low causes the STOP signal to go high, and this high is sent to the start circuitry to switch the Rebound game from the play mode to the attract mode.

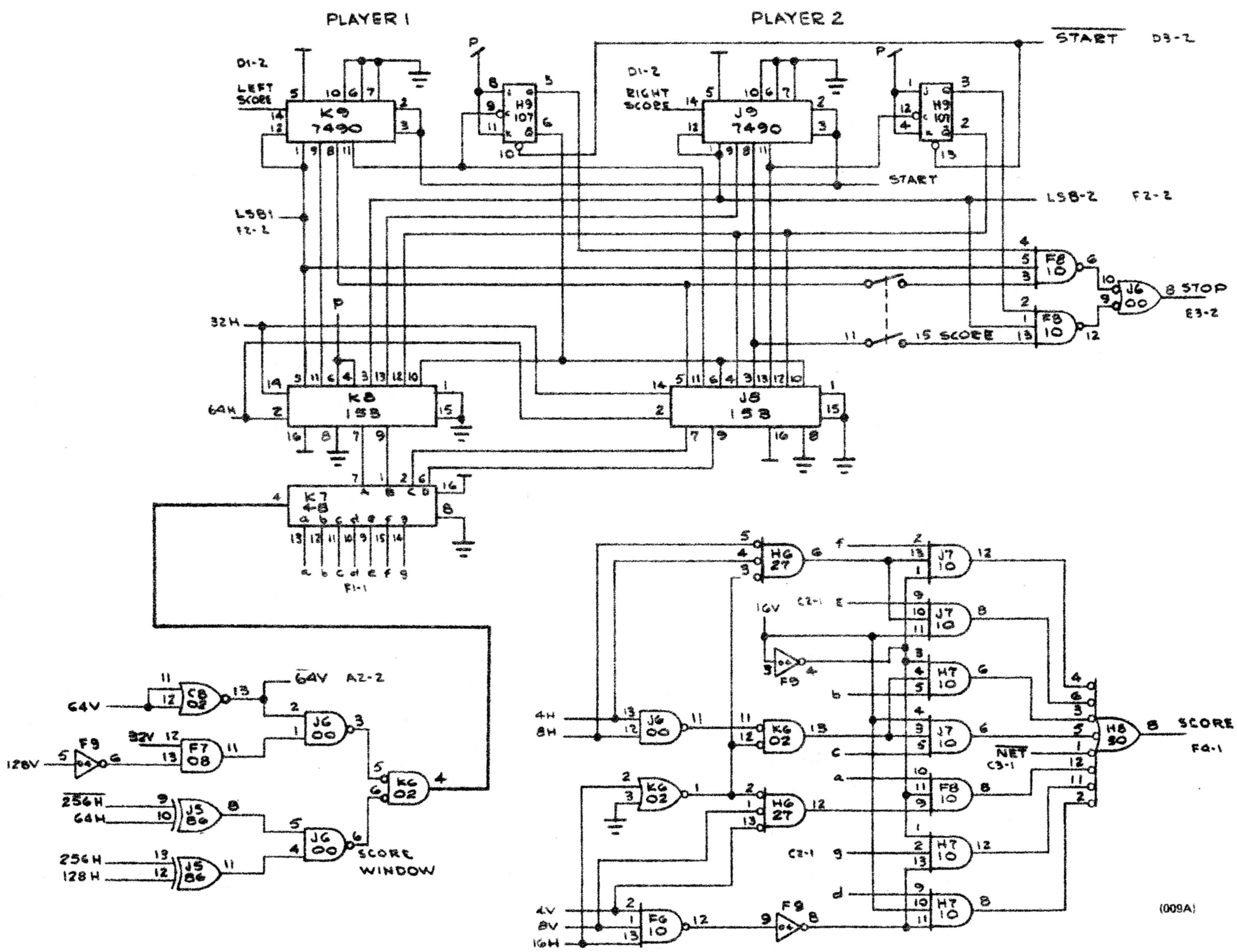


Figure 2-7. Score Circuit

2-45. PADDLE CIRCUIT

2-46. The paddle circuit (Figure 2-8) consists of two rotary potentiometers (not shown); timers C9 and B9 and associated circuitry; NOR gates C8-4 and C8-10; NAND gates D7-11, B8-6, D7-8, B8-8, H2-8, B1-11, F6-6, and F6-8; inverter B5-2; negative-true AND gate K6-10; AND gate E5-8; negative-true OR gates F7-6 and F7-8; counters C7 and B7; and multiplexer B6. Both rotary potentiometers are mounted on the front panel and are used by the players to position the paddle symbols shown on the picture tube. All other components of the paddle circuitry are located on the computer board. The paddle circuitry is subdivided into five circuits: the paddle 1 circuit, the paddle 2 circuit, the multiplexer, the paddle window circuit, and the stop circuit. Each of these circuits is described in the following text.

2-47. Paddle Window Circuit: The paddle window circuit consists of NAND gates H2-8 and B1-11, negative-true AND gate K6-10, and AND gate E5-8. Vertical timing signals 64V, 32V, 128V, 16V, and 8V are logically combined to develop a horizontal window for the paddle 1 and paddle 2 circuits. The window is located between vertical positions 248V and 256V. In addition, a 4V signal is used to gate the DISP PAD COMP (display paddle composite) signal through AND gate E5-8. Consequently, the final paddle signal is confined between vertical positions 252V and 256V.

2-48. Multiplexer: Multiplexer B6 is controlled by the 256H signal from the horizontal sync circuit. Between the leading edge of horizontal blanking and horizontal position 256H (essentially the left half of the picture), the multiplexer passes information from the paddle 1 circuit. From

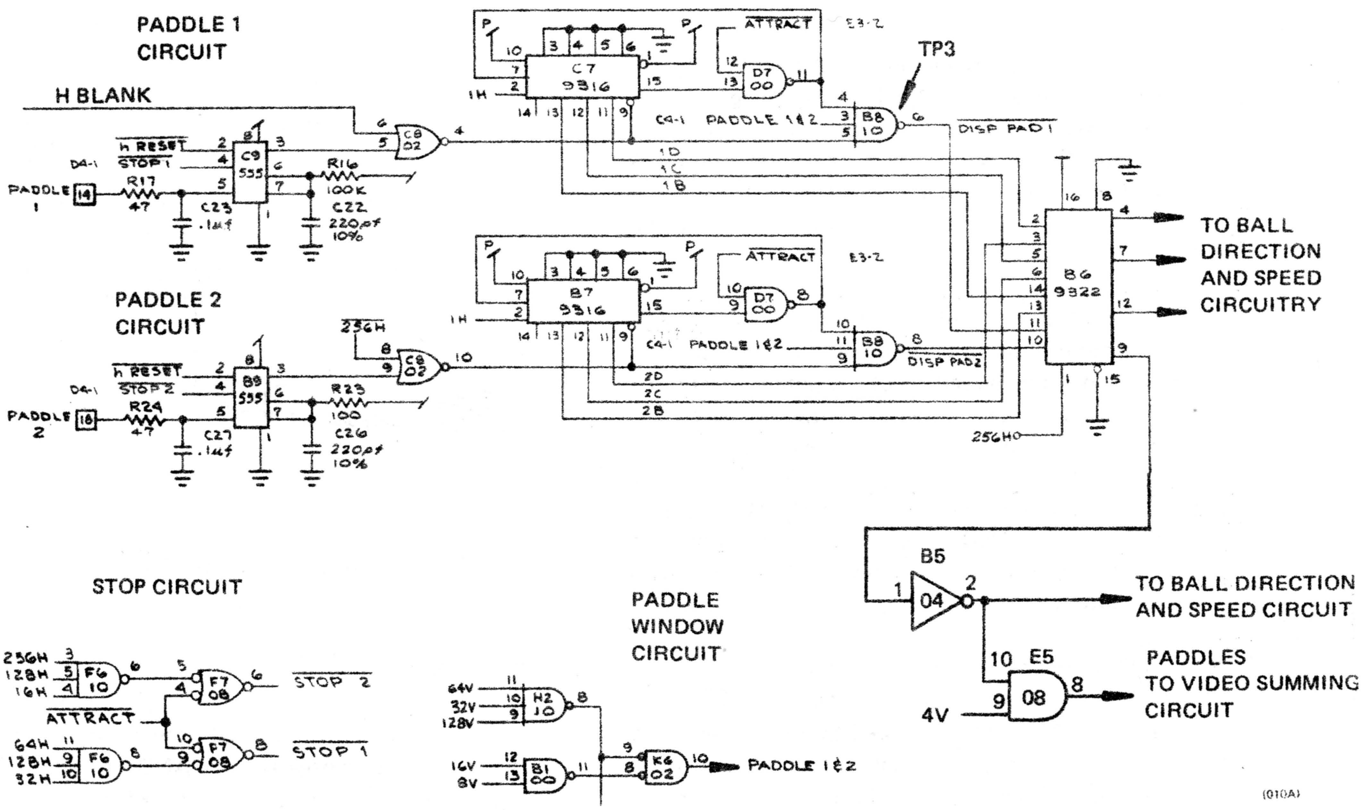


Figure 2-8. Paddle Circuit

horizontal position 256H to 453H (right half of picture), the multiplexer passes information from the paddle 2 circuit.

2-49. Paddle 1 and 2 Circuits During Attract Mode: The paddle 1 circuit consists of the front panel player 1 potentiometer; timer C9 and associated circuitry, NOR gate C8-4; counter C7; and NAND gates D7-11 and B8-6. The paddle 2 circuit consists of timer B9; NOR gate C8-10; counter B7; and NAND gates D7-8 and B8-8. Although controlled differently, these two paddle circuits operate identically.

2-50. During the attract mode, a low $\overline{\text{STOP 1}}$ signal from the stop circuit turns off timer C9 (pin C9-3 low) and a low $\overline{\text{ATTRACT}}$ signal from the start circuit inhibits NAND gate D7-11. As a result, the outputs of NOR gate C8-4 and NAND gate D7-11 are forced high during the active portion of the picture. With pins 10, 7, and 9 of counter C7 held high, it continuously counts 1H pulses and furnishes count information to multiplexer B6. When the PADDLE 1 & 2 signal is high, NAND gate B8-6 furnishes a low $\overline{\text{DISP PAD 1}}$ (display paddle 1) signal to the multiplexer. During horizontal blanking, the output of NOR gate C8-4 is forced low by the H BLANK signal. This low initializes counter C7 (zero output) and inhibits the $\overline{\text{DISP PAD 1}}$ signal. Between horizontal positions 256H and 400H the paddle 2 circuit furnishes count information and a $\overline{\text{DISP PAD 2}}$ signal to the multiplexer. Counter B7 is initialized and the $\overline{\text{DISP PAD 2}}$ signal is inhibited when the 256H signal goes high. Thus, the paddle 2 circuit does not furnish any useful information to the multiplexer for the left side of the picture.

2-51. Multiplexer B6 continuously passes first the paddle 1 information and then the paddle 2 information to the ball direction and speed circuitry and to inverter B5-2. The ball direction and speed circuitry (discussed elsewhere in this manual) receives information from counters C7 and B7, and inverter B5-2 alternately receives the low $\overline{\text{DISP PAD 1}}$ and $\overline{\text{DISP PAD 2}}$ signals. Consequently, during the active picture time, the output of inverter B5-2 is held high. When the 4V signal and the PADDLE 1 & 2 signals coincide, the DISP PAD COMP (display paddle composite) signal is passed through AND gate E5-8 to the video summing circuit. Thus, during the attract mode, a white bar, which is positioned between vertical positions 252V and 256V, is displayed from the left to right side of the picture.

2-52. Paddle 1 and 2 Circuits During Play Mode: During the play mode, a high $\overline{\text{STOP 1}}$ signal from the stop circuit enables timer C9 and a high $\overline{\text{ATTRACT}}$ signal from the start circuit enables NAND gate D7-11. Timer C9 is triggered by a negative-going $\overline{\text{H RESET}}$ pulse at the beginning

of horizontal blanking, forcing pin 3 of the timer high. This high, in conjunction with a high H BLANK signal, forces the output of NOR gate C8-4 low, which initializes counter C7 and inhibits NAND gate B8-6. When horizontal blanking is ended, pin 6 of NOR gate C8-4 goes low allowing timer C9 to control the gate for the remainder of the horizontal line.

2-53. The time constant of timer C9 is controlled by the front panel paddle position potentiometer. When C9 times out, as determined by the setting of the potentiometer, pin 3 of the timer goes low forcing the output of NOR gate C8-4 high. As a result, counter C7 begins counting 1H pulses and furnishes the resulting count information to the multiplexer. In addition, the high output of NOR gate C8-4 enables pin 5 of NAND gate B8-6. Thus, when the PADDLE 1 & 2 signal goes high, a low $\overline{\text{DISP PAD 1}}$ signal is sent to the multiplexer.

2-54. Multiplexer B6 passes the output of counter C7 to the ball direction and speed circuitry and the $\overline{\text{DISP PAD 1}}$ signal to inverter B5-2. When allowed by the 4V signal, the high output of inverter B5-2 is sent to the television monitor via AND gate E5-8 to cause the paddle 1 symbol to appear on the picture tube. When counter C7 reaches the count of BCD 1111 (decimal 15), pin 15 of the counter goes high and forces the output of NAND gate D7-11 low. This low stops the counter and inhibits NAND gate B8-6, causing the right edge of the paddle 1 symbol to be formed. Thus, the paddle 1 circuit determines where the left edge of paddle 1 starts on the TV screen and terminates the paddle symbol 15 1H pulses later. Using the front panel paddle 1 potentiometer in the play mode, the paddle 1 symbol can be moved back and forth horizontally between the left side and approximately the vertical center of the TV picture. The paddle 2 circuitry operates approximately the same as the paddle 1 circuit. However, the paddle 2 symbol cannot begin until the $\overline{\text{256H}}$ signal applied to NOR gate C8-10 goes low and the 256H signal applied to multiplexer B6 goes high. The right travel of both paddle symbols is limited by the stop circuit.

2-55. **Stop Circuit:** The stop circuit is composed of NAND gates F6-6 and F6-8 and negative-true OR gates F7-6 and F7-8. When the electron beam of the picture tube reaches horizontal position 224H during the play mode, the output of NAND gate F6-8 goes low. This low is passed through gate F7-8 to timer C9, causing pin 3 of the timer to go high and forcing the output of NOR gate C8-4 low. Consequently, counter C7 is reset to zero and NAND gate B8-6 is inhibited and paddle 1 symbol information is prevented from being displayed after horizontal position 224H. In a similar manner, paddle 2 information from the paddle 2 circuit is suppressed after horizontal position 400H.

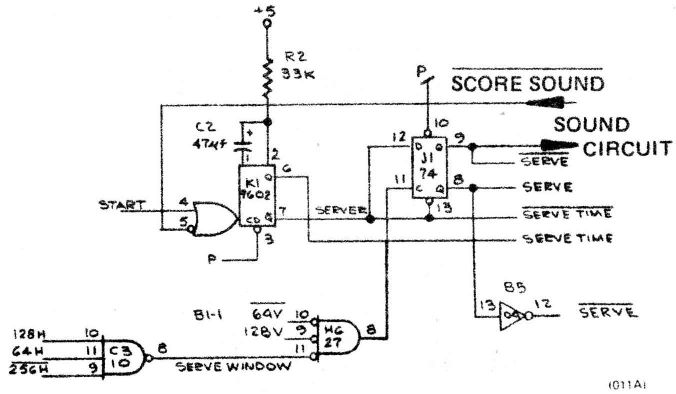


Figure 2-9. Serve Circuit

2-56. SERVE CIRCUIT

2-57. As shown in Figure 2-9, the serve circuit consists of NAND gate C3-8; negative-true AND gate H6-8; one-shot K1-6/7; flip-flop J1-9/8; and inverter B5-12. This circuit is used to generate the SERVE, $\overline{\text{SERVE}}$, SERVE TIME, and $\overline{\text{SERVE TIME}}$ signals that cause the horizontal and vertical ball motion circuits to initiate a serve after the front panel start pushbutton is pressed to start a new game, after each time the ball symbol goes out of bounds, or after the ball symbol hits a paddle four times without crossing the net. The serve circuit consists of a serve window circuit and a timing circuit, which are discussed in the following paragraphs.

2-58. **Serve Window Circuit:** NAND gate C3-8 and negative-true AND gate H6-8 form the serve window circuit. This circuit logically combines the 128H, 64H, $\overline{\text{256H}}$, $\overline{\text{64V}}$, and 128V signals from the horizontal sync and vertical sync circuits to develop a serve window that is located between vertical positions 64V and 128V and between horizontal positions 196H and 256H. The positive-going window pulse developed at the output of gate H6-8 is used to clock flip-flop J1-9/8 of the timing circuit.

2-59. **Timing Circuit:** The timing circuit consists of one-shot K1-6/7, flip-flop J1-9/8, and inverter B5-12. When the front panel start pushbutton is pressed after game credit has been established, the START signal goes high. This high START signal triggers one-shot K1-6/7, causing it to develop a nominal 0.5 second positive-going pulse at pin 6 (SERVE TIME) and a 0.5 second negative-going pulse at pin 7 ($\overline{\text{SERVE TIME}}$). One-shot K1-6/7 is also triggered whenever the ball goes out of bounds or after the ball hits a

paddle four times without crossing the net by a negative-going pulse from the sound circuit. In either case, the SERVE TIME pulse is sent to various circuits of the computer, and the $\overline{\text{SERVE TIME}}$ pulse is sent to the D and clear inputs of flip-flop J1-9/8 and to the ball direction and speed circuit. Flip-flop J1-9/8 is cleared by the negative-going $\overline{\text{SERVE TIME}}$ pulse, causing its Q output ($\overline{\text{SERVE}}$) to go low and its $\overline{Q}$ output (SERVE) to go high. After one-shot K1-6/7 times out, pin 6 of K1 goes low and pin 7 goes high. When the next positive-going serve window signal appears at the output of gate H6-8, the high $\overline{Q}$ output of one-shot K1-6/7 causes the Q output of flip-flop J1-9/8 to go high and the $\overline{Q}$ output to go low. The high $\overline{\text{SERVE}}$ signal from the Q output is sent to the sound circuit, net circuit, and to the ball direction and speed circuit. The low SERVE output is sent to the out-of-bounds/fourth-hit circuit and to inverter B5-12. The high $\overline{\text{SERVE}}$ output of inverter B5-12 is sent to the horizontal ball motion circuit.

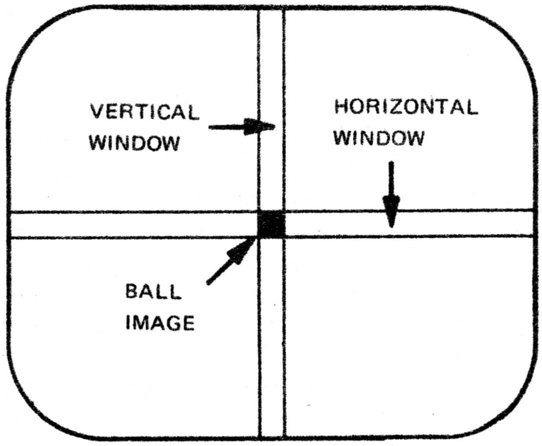
2-60. BALL MOTION

2-61. The ball image is created by intensifying the TV display at the intersection of narrow horizontal and vertical windows (Figure 2-10a). The two windows are moved independent of each other by the ball direction and speed circuits. When the horizontal and vertical windows move at the same speed (Figure 2-10b), the ball will appear to travel across the display at a 45° angle. A faster vertical window speed (Figure 2-10c) will cause the ball to move faster in the horizontal direction and vice versa.

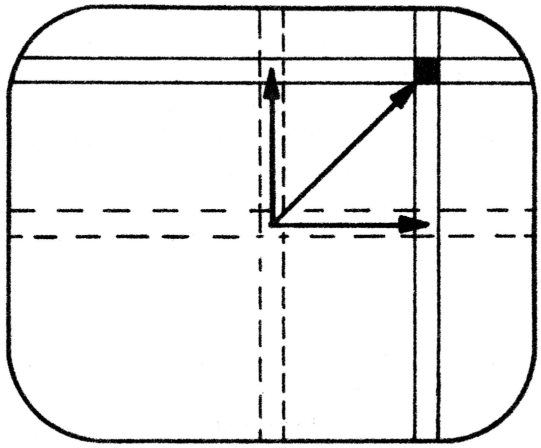
2-62. HORIZONTAL BALL MOTION

2-63. The horizontal ball motion circuit is almost identical in construction to the horizontal synchronization circuit. The major difference between the two circuits is that the counting process of the horizontal ball motion circuit can be controlled and it is this fact that is used to produce a counting differential between the sync circuit counting and the counting of the horizontal motion window.

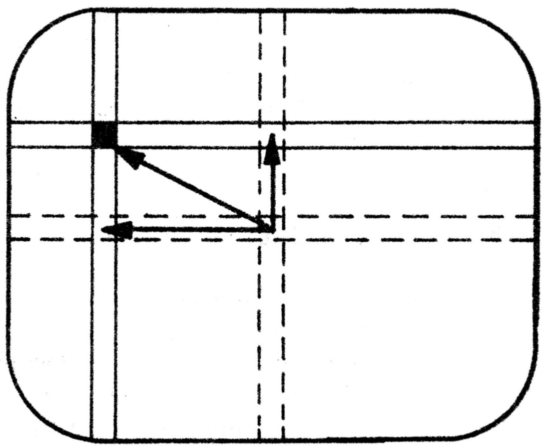
2-64. This counting differential is used to create a window that has the appearance of moving across the CRT screen. If the window is created in a slightly different place during each TV field, the window appears to move in much the same way the illusion of movement is created on the movie screen by the film in the motion picture projector. Even though ball motion consists only of a series of shifted ball images, the illusion of motion results from a combination of persistence of the image on the CRT phosphor and the persistence of the retinal after-image in the human eye. Thus, the human eye, unable to cope with the speed the



a. Ball Still



b. Equal Window Speeds



c. Faster Vertical Window

Figure 2-10. Ball Image Generation

ball image is shifted, interprets the information as real movement.

2-65. If the ball window signal occurs at the same frequency as the sync signal, the window appears in the same place each TV field. However, if the window signal that produces horizontal ball motion is delayed so that it counts one more clock pulse than horizontal sync, the window created in the next field is shifted one clock pulse to the right. If the signal is delayed yet another pulse, the resultant ball window is shifted two clock pulses to the right of the original position. The TV monitor electron beam sweeps 60 fields per second. If the vertical window is shifted one clock pulse per field, the ball will appear to move quite rapidly in the horizontal plane.

2-66. Horizontal ball motion direction is dependent on whether the horizontal motion signal is counted faster or slower than the horizontal sync signal. If it is counted at a faster rate (less clock pulses), the ball window will move left. If it is counted slower (more pulses), the window will move to the right. If it is counted at the same rate, the window does not shift either way. The velocity of the window motion is controlled by varying the distance the window is shifted per TV field. If the window is shifted one clock pulse per field, it appears to move half as fast as if it were shifted two clock pulses per field.

2-67. The horizontal motion circuit uses 9316 counters, which are almost identical to the 7493 counters of the horizontal sync circuit; the counters of both circuits are run in parallel by the same clock. The 7493 counters always start counting from zero. The count of the 9316, however, is started from a predetermined number. This predetermined number is generated by the ball direction and speed circuit and is known as the motion code. It is this binary motion code that produces the shift differential between the horizontal sync counting and the counting of the horizontal ball motion circuit.

2-68. VERTICAL BALL MOTION

2-69. The vertical ball motion circuit is almost identical to the horizontal motion circuit with the following exceptions. This circuit creates a horizontal window that moves vertically and, therefore, different inputs are used. The electron beam is blanked out during its vertical retrace, so $\overline{\text{V BLANK}}$ is used to turn the electron beam on and off at the right times. $\overline{\text{H SYNC}}$ provides the clock for the counters so that the horizontal window is created after the right number of horizontal lines. This circuit does not use a J-K flip-flop as a ninth bit for the counter because the largest number it needs to count is 272. The horizontal motion counters need to count to 455.

2-70. BALL DIRECTION AND SPEED CIRCUIT

2-71. The ball direction and speed circuit (Figure 2-11) consists of flip-flops D6-5, C6-5, D6-9/8, and C6-9/8; counter B4; up/down counter E4; exclusive OR gates C5-6, C5-3, C5-11, and C5-8; NAND gates D5-3, D5-8, and D5-11; negative-true AND gate E6-10; negative-true OR gates E5-6 and E5-11; and inverter B5-6. This circuit processes paddle, ball, serve, and score information and sends ball direction and speed information to the horizontal and vertical ball motion circuits.

2-72. Just prior to the actual serve initiation ($\overline{\text{SERVE}}$ signal going high), the $\overline{\text{SERVE TIME}}$ signal from the serve circuit goes low. This low signal clears flip-flop D6-5, causing the $\overline{\text{BACKWARDS}}$ signal to go low. A low $\overline{\text{BACKWARDS}}$ in the presence of no score directs the horizontal ball motion circuit to move the ball toward the right side of the TV picture when one-shot K1-6/7 of the serve circuit times out.

2-73. At the time of the initial serve in a game, the left player and right player scores are zero. Thus, the least significant bit signals (LSB-1 and LSB-2) from the score counters are both low and these lows force the output of exclusive-OR gate C5-8 to be low also. This low inhibits NAND gate D5-8 and is inverted by inverter B5-6 to form a high that enables NAND gate D5-11. Because the $\overline{\text{SERVE}}$ signal is also high at this time, the output of NAND gate D5-11 is forced low to clear flip-flops C6-5 and C6-9/8 and preset flip-flop D6-9. Consequently, the Q outputs of flip-flops C6-5 and C6-9/8 are low, the Q output of flip-flop D6-9/8 is high, the $\overline{Q}$ output of flip-flop D6-9/8 is low, and the $\overline{Q}$ output of flip-flop C6-9/8 is high.

2-74. The low output (signal DP) of flip-flop C6-5 is sent to the horizontal ball motion circuit and to exclusive OR gates C5-3 and C5-11. The high output (signal CP) of flip-flop D6-9/8 is applied to exclusive OR gate C5-3, and the low output (signal $\overline{\text{CP}}$) is sent to the horizontal ball motion circuit. The low output (signal BP) of flip-flop C6-9/8 is applied to exclusive OR gate C5, and the high output (signal $\overline{\text{BP}}$) is sent to the horizontal ball motion circuit. As a result, gate C5-3 furnishes a high level to negative-true OR gate E5-6, and gate C5-11 furnishes a low level to pin 15 of up/down counter E4. At the same time flip-flops C6-5, D6-9/8, and C6-9/8 are being cleared or preset, the $\overline{\text{SERVE}}$ signal from the serve circuit is low. Consequently, a low level is applied to pin 10 of counter E4 and to gate E5-6. In

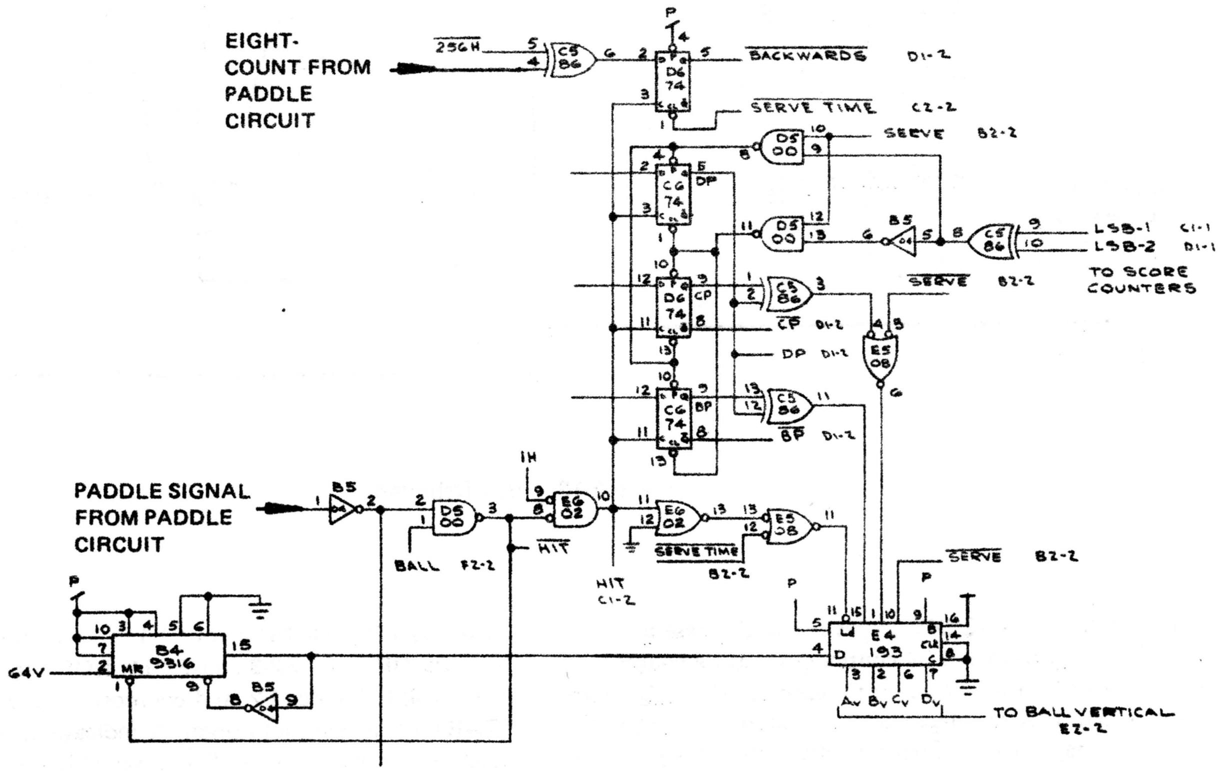


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Figure 2-11. Ball Direction and Speed Circuit

turn, gate E5-6 furnishes a low level to pin 1 of counter E4. Because the $\overline{\text{SERVE TIME}}$ signal from the serve circuit is also low at the same time the $\overline{\text{SERVE}}$ signal is low, the levels at the preset inputs (pins 15, 1, 10, and 9) are loaded into counter E4 by the low output of gate E5-11. These preset levels represent a BCD 1000 (decimal 8), which is furnished via signals D_V, C_V, B_V, and A_V to the vertical ball motion circuit. This preset count is modified by a signal from the gravity simulator (counter B4), which is discussed in subsequent text.

2-75. During game play, three bits of BCD information from the multiplexer of the paddle circuit are regularly supplied to flip-flops C6-5, D6-9/8, and C6-9/8 of the ball direction and speed circuitry. This information indicates what portion (if any) of each paddle is present at each horizontal position of a horizontal line. Each time the ball "strikes" a paddle, pin 2 of NAND gate D5-3 is high (indicating the presence of a paddle), and the BALL signal from the horizontal and vertical ball motion circuits is high (indicating the presence of the ball). These highs force the output of NAND gate D5-3 low and this low $\overline{\text{HIT}}$ signal resets counter B4, enables negative-true AND gate E6-10, and is sent to the sound circuit to cause a hit sound to be generated.

2-76. When the next 1H pulse goes low, the output of gate E6-10 goes high (HIT signal). This high HIT signal causes the paddle segment information from the paddle circuit to be clocked into flip-flops C6-5, D6-9/8, and C6-9/8; is sent to the out-of-bounds/fourth hit/net hit circuit to record a hit; and is applied to NOR gate E6-13. The paddle segment information appearing at the outputs of flip-flops C6-5, D6-9/8, and C6-9/8 is sent to the horizontal ball motion circuit and via gating to the preset inputs of up/down counter E4. The high HIT signal is inverted by NOR gate E6-13 and then passed through negative-true OR gate E5-11 to pin 11 of counter E4, causing the preset information at pins 15, 1, 10, and 9 to be loaded into the counter.

2-77. Upon being reset to zero by the $\overline{\text{HIT}}$ signal, counter B4 begins accumulating 64V pulses. After 15 64V pulses have been accumulated, pin 15 of counter B4 goes high. This high causes counter E4 to be down counted one count from the preset value, which is determined by the outputs of gates C5-11 and E5-6, a high $\overline{\text{SERVE}}$ signal, and a fixed positive level. In addition, inverter B5-8 inverts the high output at pin 15 of counter B4, causing a fixed preset value (BCD 0011) to be loaded into the counter. Thus, until the next hit is sensed, the counter develops a high pulse

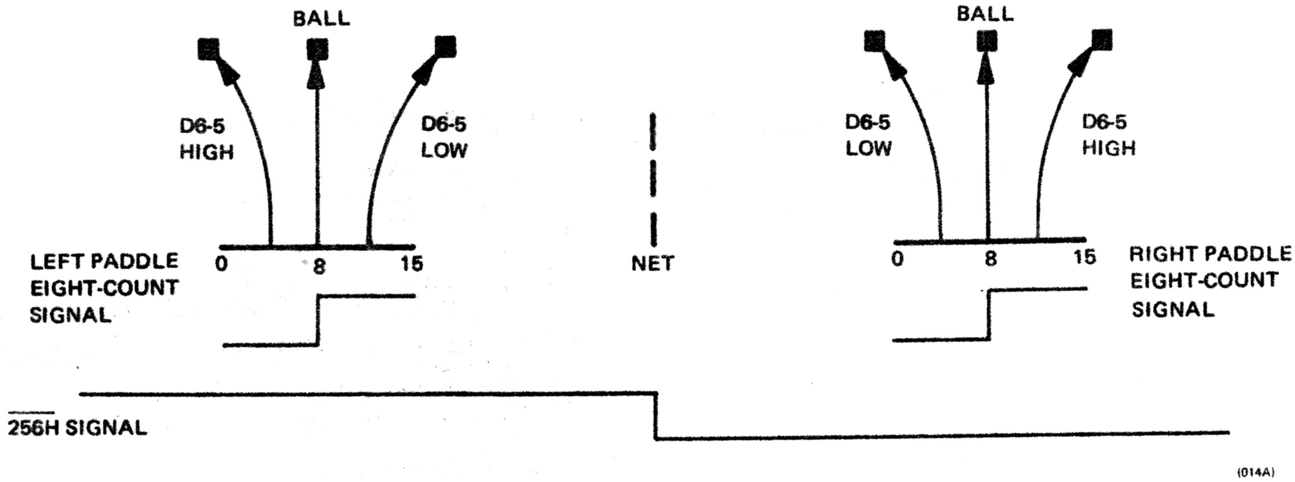


Figure 2-12. Ball Rebound

at pin 15 for every 12 64V pulses received. These positive-going pulses at pin 15 of B4 continuously cause counter E4 to be counted down one count for each positive pulse from counter B4. This technique of down counting counter E4 simulates the effect of gravity on the vertical travel of the ball. Thus, the ball symbol is caused to move in a ballistic trajectory across the screen of the picture tube.

2-78. Whenever the score is unequal during the game, the output of exclusive OR gate C5-8 is high. This high enables NAND gate D5-8 and causes NAND gate D5-11 to be inhibited. Consequently, the preset/clear configuration of flip-flops C6-5, D6-9/8, and C6-9/8 is caused to be different from the configuration caused by an equal score. This different preset/clear configuration causes a different speed code preset to be loaded into counter E4. As a result, the vertical serve speed is altered as the score changes.

2-79. Exclusive OR gate C5-6 and flip-flop D6-5 function together to cause the ball to move in various directions, depending on where the ball is hit on which paddle. The eight count in each paddle circuit, which indicates the approximate center of the paddle, is exclusively ORed with the $\overline{256H}$ signal in gate C5-6. Each time the HIT signal occurs, the output of gate C5-6 is clocked into flip-flop D6-5. Figure 2-12 depicts the direction of travel of the ball in various situations.

2-80. HORIZONTAL BALL MOTION CIRCUIT

2-81. Figure 2-13 shows the circuitry of the horizontal ball motion circuit. This circuit is composed of flip-flops F1-6 and F3-3; NAND gates E1-11, C3-6, and F4-8; negative-true OR gates F2-3 and F2-11; NOR gate H1-8; AND gate F2-6; full adder E2; and counters E3 and D3. When a START command, out-of-bounds indication, fourth-hit indication is sensed, a low $\overline{\text{SERVE}}$ signal is developed, causing counters E3 and D3 to be reset and flip-flop F3-3 to be cleared (Q output low). At the same time, a low $\overline{\text{SERVE TIME}}$ signal causes the $\overline{\text{BACKWARDS}}$ signal to go low, which causes the $\overline{\text{Q}}$ output of flip-flop F1-6 to go high. When the V RESET signal goes high, just prior to the beginning of a new field, flip-flop F1-6 is clocked and AND gate F2-6 furnishes a high level to gates F2-3, F2-11, and H1-8. This high level allows these gates to pass horizontal speed information (signals $\overline{\text{BP}}$, $\overline{\text{CP}}$, $\overline{\text{DP}}$, and DP) to the inputs of full adder E2. The horizontal speed information and a fixed zero at pin E2-1 is summed with three bits of fixed information (ones at pins E2-4 and E2-7 and a zero at pin 16) and the DP signal. The resulting sum is sent to the preset inputs of counter E3.

2-82. When the $\overline{\text{SERVE}}$ signal goes high, counters E3 and D3 begin counting CLOCK pulses and flip-flop F3-3 is allowed to be toggled. At the count of 226 (approximately half a horizontal line), pin 15 of counters E3 and D3 and pin 3 of flip-flop F3-3 are high, causing NAND gates C3-6 and F4-8 to be enabled. Enabling NAND gate F8-8 causes a low $\overline{\text{H VIDEO}}$ signal to be sent to the ball motion summing circuit to cause the ball to appear at the vertical center of the TV picture. Enabling NAND gate C3-6 causes the ball speed preset data to be loaded into counter E3 and the fixed preset data (BCD 0011) to be loaded into counter D3. These presets cause the vertical window to be displaced a fixed amount to the right of center of the display for each

new field that is painted, thus providing the horizontal speed vector of the ball during the serve. Notice that the Q output of flip-flop F3-3 is toggled low at the end of the second half line count and is then toggled high after a full line count (including presets). Consequently, the low $\overline{\text{BALL LOAD}}$ and $\overline{\text{H VIDEO}}$ are now developed once per line until the next serve.

2-83. If the ball hits the right half of the left paddle or the left half of the right paddle, a low $\overline{\text{BACKWARDS}}$ signal clears flip-flop F1-6. Therefore, gates F2-3, F2-11, and H1-8 are enabled during the next V RESET signal. However, in this instance, the speed data applied to adder E2 depends on where the ball "strikes" the paddle. As a result, the horizontal ball motion circuit develops a vertical window that moves at a rate determined by the speed data present at the inputs of gates F2-3, F2-11, and H1-8.

2-84. If the ball hits the left half of the left paddle or the right half of the right paddle, a high $\overline{\text{BACKWARDS}}$ signal is applied to pin 1 of flip-flop F1-6. Thus, the $\overline{Q}$ output of flip-flop F1-6 remains low, which inhibits F2-6. Inhibiting gate F2-6 causes a BCD 0100 to be summed with a BCD 0110 in the adder (E2) to yield a BCD 1010, which is a preset code that causes the horizontal ball motion circuit to move the vertical window at full horizontal speed.

2-85. If the ball hits the center of the paddle (count seven of the paddle counter), the circuit composed of flip-flop F1-6 and AND gate F2-6 allows speed data to pass through gates F2-3, F2-11, and H1-8 when the V RESET signal goes high. When this data and a fixed zero at pin E2-1 is summed with signal DP and fixed inputs of adder E2, a stop code (0101) appears at the output of the adder. When the stop code is preset into counter E3, the ball motion counter (E3, D3) counts in synchronism with beam

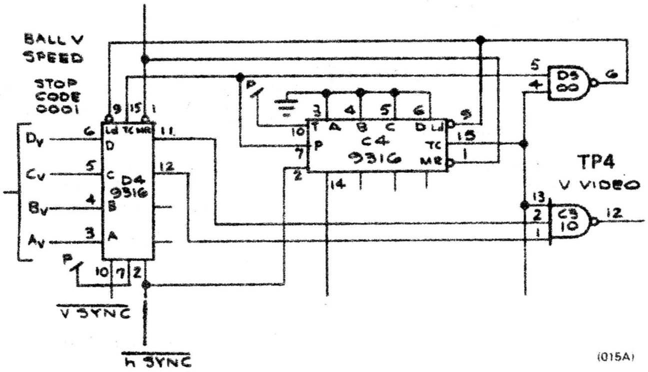


Figure 2-14. Vertical Ball-Motion Circuit

sweep, which results in no horizontal motion. With no horizontal speed vector, the ball is moved straight up and down by the vertical ball motion circuit.

2-86. VERTICAL BALL MOTION CIRCUIT

2-87. The vertical ball motion circuit (Figure 2-14) is composed of counters D4 and C4 and NAND gates D5-6 and C3-12. This circuit is similar to the horizontal ball motion counter (E3, D3, F3-3, C3-6, and F4-8).

2-88. When the $\overline{\text{SERVE}}$ signal from the serve circuit goes low, counters D4 and C4 are reset. When the $\overline{\text{SERVE}}$ signal goes high indicating a serve is to be initiated and the $\overline{\text{V SYNC}}$ signal goes high indicating the beginning of a new field, counters D4 and C4 begin accumulating $\overline{\text{H SYNC}}$ pulses. After 225 counts (approximately one field), NAND gates D5-6 and C3-12 are enabled, causing a low V VIDEO signal to be sent to the ball motion summing circuit to cause a horizontal window and counter D4 to be preset with vertical ball motion data for the serve.

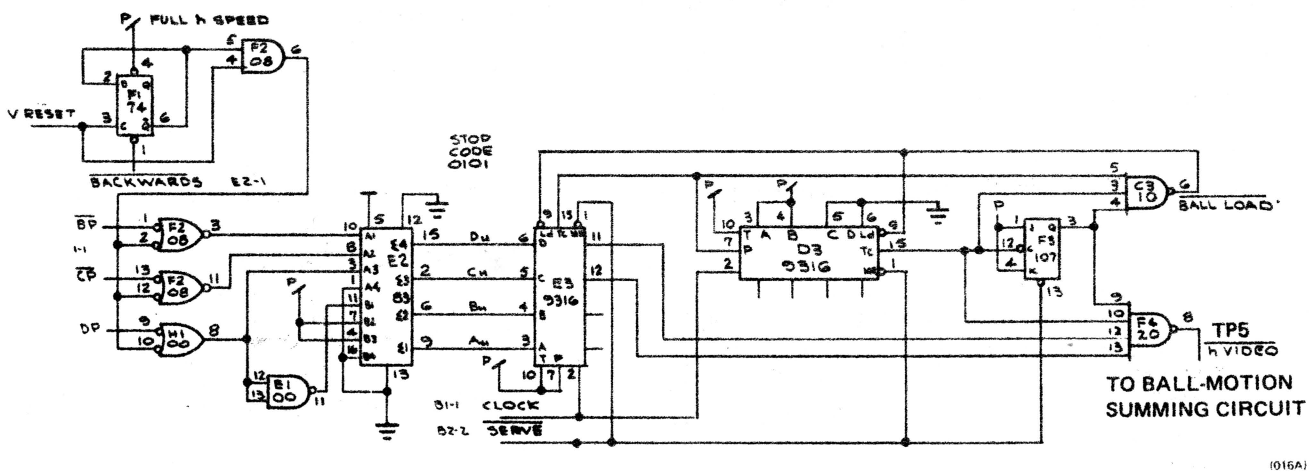


Figure 2-13. Horizontal Ball-Motion Circuit

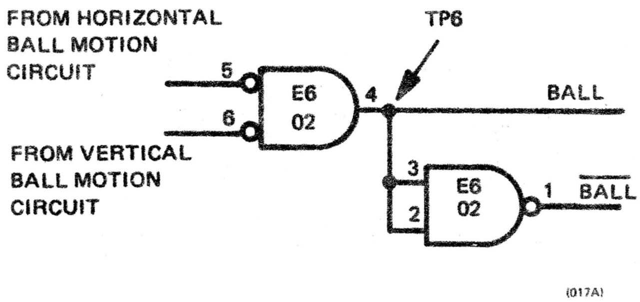


Figure 2-15. Ball Motion Summing Circuit

2-89. When the ball hits a paddle, new ball speed data is furnished to the preset inputs of counter D4. Thus, the horizontal window is caused to be moved up and down at a rate determined by the new speed data. The terminal count signal and the LSB signal of counter C4 are sent to the sound circuit. These signals help develop the sound that accompanies a hit or score.

2-90. BALL MOTION SUMMING CIRCUIT

2-91. The ball motion summing circuit (Figure 2-15) is composed of negative-true AND gate E6-4 and a NOR gate E6-1 that is used as an inverter. When the H VIDEO signal (vertical ball window) and V VIDEO (horizontal ball window) are coincidently low, a high BALL signal is sent to NOR gate E6-1 and the out-of-bounds/fourth hit/net hit circuit.

2-92. VIDEO SUMMING CIRCUIT

2-93. Figure 2-16 shows the video summing circuit, which is composed of capacitor C25 and resistors R25 through R29. This circuit combines the SCORE, $\overline{\text{COMPOSITE SYNC}}$, BALL, and PADDLES signals into a composite VIDEO OUT signal. Capacitor C25 couples the VIDEO OUT signal to the video circuits of the TV monitor.

2-94. OUT-OF-BOUNDS/FOURTH HIT/NET HIT CIRCUIT

2-95. The out-of-bounds/fourth hit/net hit circuit (Figure 2-17) consists of flip-flops B3-3, J2-5, and B2-5/6; counter C1; one-shot D1-9; negative-true OR gate B1-8; exclusive OR gate J5-3; AND gates E5-3, A1-11, and A1-3; NOR gates D2-10 and D2-1; negative-true AND gates D2-4 and D2-13; and AND-OR-INVERT gates C2-8 and C2-6. This circuit senses when the ball has hit a paddle four times; has gone out of bounds at the top, bottom, or either side of the picture; or has hit the net. If the ball is missed by a paddle, the miss is sensed when the ball goes out of bounds at the bottom of the picture. When the ball goes out of bounds, hits a paddle four times, or hits the net, a signal is sent to the sound circuit to cause a score sound; and another signal is sent to the score circuit to cause the appropriate score to be displayed.

2-96. Just prior to the ball being served, the $\overline{\text{SERVE}}$ signal goes low, which clears flip-flop B3-3 and presets flip-flop J2-5. With the Q output of flip-flop B3-3 low and the Q output of flip-flop J2-5 high, exclusive OR gate J5-3 passes a high level that resets counter C1. When the next positive-going 2H pulse occurs, the Q output of flip-flop J2-5 is clocked low, which inhibits exclusive OR gate J5-3.

2-97. When the ball is served, the BALL signal goes high. Since the ball is served to the right player, the 256H signal is high at this time. As a result, the Q output of flip-flop B3-3 goes high, which causes another high reset pulse to be applied to counter C1. The high at the Q output of flip-flop B3-3 is clocked to the Q output of flip-flop J2-5 when the next positive-going 2H pulse occurs. Consequently, the output of exclusive OR gate J5-3 goes low, thereby enabling counter C1.

2-98. If a hit occurs, one-shot D1-14 is triggered by a positive-going HIT SOUND pulse and generates a negative-going pulse that increments counter C1 one count. If the ball is subsequently hit by the left paddle, flip-flop B3-3 changes states and exclusive OR gate J5-3 passes a high level that resets counter C1. If the ball goes out of bounds or hits the net, flip-flop B3-3 also is forced to change state by the next low $\overline{\text{SERVE}}$ signal, causing counter C1 to be reset. However, if the ball hits the right paddle four times without being hit with the left paddle, hitting the net, or going out of bounds, pin 8 of counter C1 goes high (4TH HIT signal). This high is applied to NOR gate D2-10.

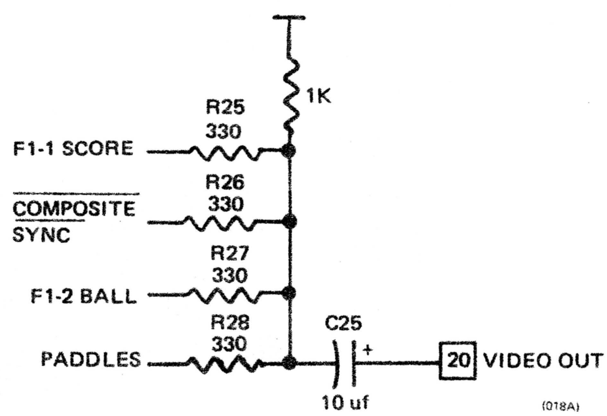


Figure 2-16. Video Summing Circuit

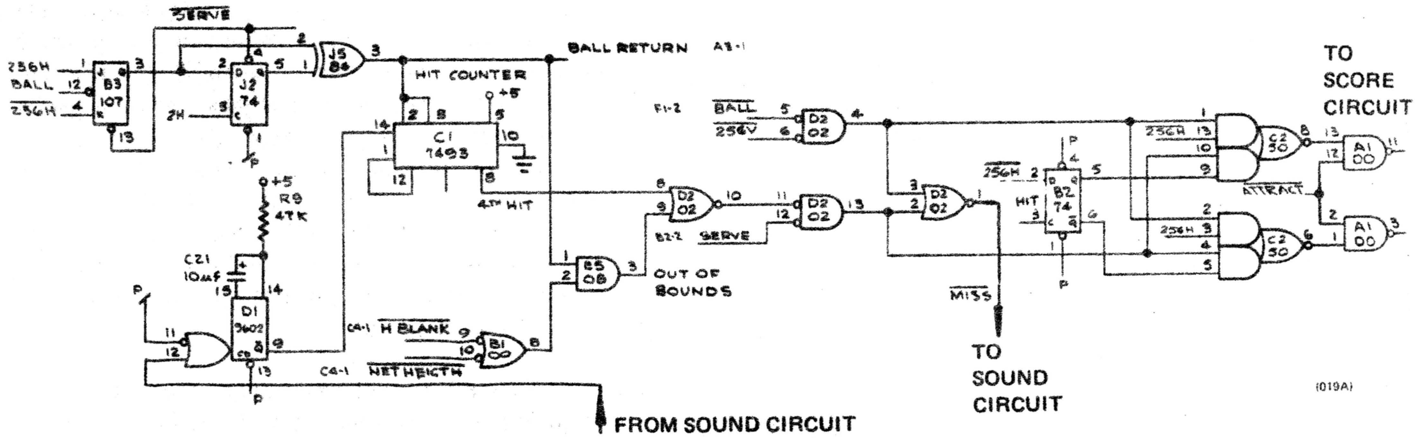


Figure 2-17. Out-of-Bounds/Fourth-Hit/Net-Hit Circuit

2-99. When horizontal blanking occurs (as indicated by H BLANK signal) or the net symbol is being developed (as indicated by NET HEIGHT signal), the output of negative-true OR gate B1-8 is high. If either of these signals occurs coincidently with a high BALL RETURN signal (indicating ball in flight), the output of AND gate E5-3 goes high (OUT OF BOUNDS signal) to indicate the ball has either gone out of bounds at the left or right side of the picture or has hit the net.

2-100. If the ball goes out of bounds to the left or right, hits the net, or hits a paddle four times without hitting the other paddle, the output of NOR gate D2-10 goes low. If the output of gate D2-10 is low after a serve (as indicated by a low SERVE signal), the output of negative-true AND gate D2-13 goes high. This high is applied to NOR gate D2-1 and to AND-OR-INVERT gates C2-8 and C2-6.

2-101. If the ball goes out of bounds at the top or bottom of the picture, the BALL and 256V signals are simultaneously low. The resulting high output of gate D2-4 is applied to NOR gate D2-1 and to AND-OR-INVERT gates C2-8 and C2-6.

2-102. Whenever the ball goes out of bounds, hits the net, or hits a paddle four times without hitting the other paddle, a low MISS signal is developed at the output of NOR gate D2-1; and enabling levels are applied to AND-OR-INVERT gates C2-8 and C2-6. The MISS signal is sent to the sound circuit to cause a score sound to be developed. The signals applied to gates C2-8 and C2-6 are used in the development of the RIGHT SCORE and LEFT SCORE signals.

2-103. If the ball goes out of bounds at the top or bottom of the left half of the picture, pins 1 and 13 of gate C2-8 are simultaneously high, causing the output of the gate to be low. In the play mode, the ATTRACT signal is high. Therefore, AND gate A1-11 passes a negative-going pulse that is used to increment the right score by one. If the ball goes out of bounds at the top or bottom of the right half of the picture, AND gate A1-3 passes a negative-going pulse that increments the left score by one.

2-104. If the ball is hit by the left paddle, the Q output of flip-flop B2-5 is high. Consequently, if the ball goes out of bounds at the right or left side of the picture, hits the left paddle four times without hitting the other paddle, or hits the net, pins 9 and 10 of gate C2-8 are simultaneously high. As a result, gate C2-8 develops a negative-going pulse that is routed through gate A1-11 to increment the right score by one. The left score is similarly incremented if the ball is hit by the right paddle four times without hitting the left paddle, goes out of bounds at the right or left side of the picture, or hits the net. During the attract mode, the ATTRACT signal is low, which prevents gates A1-11 and A1-3 from passing score-incrementing pulses.

2-105. SOUND CIRCUITRY

2-106. One-shot D1-2/7, flip-flop F1-8, NAND gates E1-8 and E1-3, negative-true OR gate F2-8, and negative-true OR gate E1-6 form the sound circuit (Figure 2-18). This circuit sends a SOUND OUT signal to the audio circuits of the TV monitor when a paddle "hits" the ball or the ball goes out of bounds, hits one paddle four times without hitting the other paddle, or hits the net.

2-107. One-shot D1-6/7 is triggered each time the MISS signal from the out-of-bounds/fourth hit/net hit circuit goes low, indicating the ball has gone out of bounds, hit the net, or hit one paddle four times without hitting the other paddle. Triggering one-shot D1-6/7 causes a negative-going pulse to be sent to the serve circuit to initiate another serve

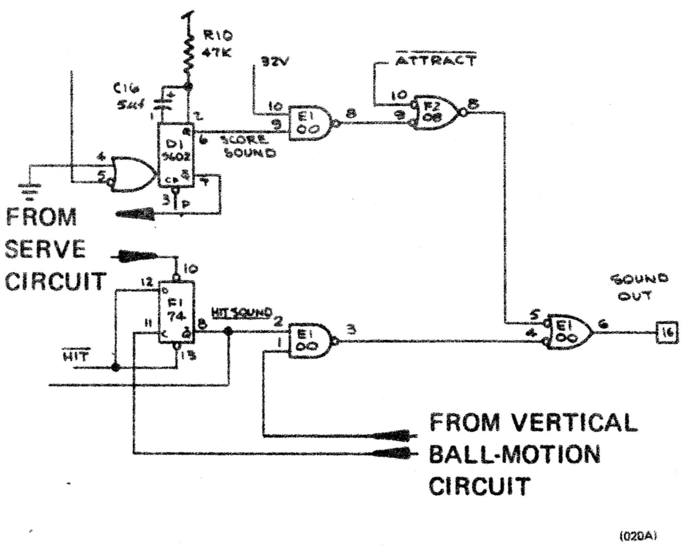


Figure 2-18. Sound Circuit

sequence and causes a positive-going pulse to be applied to NAND gate E1-8. This positive-going pulse enables gate E1-8, allowing the 32V signal to be sent to negative-true NOR gate F2-8. During the play mode. gate F2-8 is enabled by a high ATTRACT signal, allowing the 32V signal to be applied to negative-true OR gate E1-6.

2-108. When the serve sequence is initiated, a low SERVE signal presets flip-flop F1-8, which causes NAND gate E1-3 to be inhibited. When a paddle hits the ball, a negative-going HIT signal from the ball direction and speed circuit clears flip-flop F1-8, causing NAND gate E1-3 to be enabled. Upon being enabled, gate E1-3 passes a signal from the vertical ball motion circuit to gate E1-6. Later, after the HIT signal has gone high, another signal from the vertical ball motion circuit causes flip-flop F1-8 to change states, which, in turn, inhibits gate E1-3.

2-109. Negative-true OR gate E1-6 passes the periodic signal from either gate F2-8 or E1-3 to the sound circuit of the TV monitor. The sound circuit amplifies the SOUND OUT signal and provides an audible output at the speaker of the TV monitor.

2-110. NET CIRCUIT

2-111. The net circuit (Figure 2-19) consists of one-shot K1-9; flip-flops J1-5/6 and B2-8; counters K2 and K3; NAND gates H1-6, H2-8, K4-8, and B8-12; negative-true OR gate K4-6; and inverter B5-10. This circuit develops the signal for the net symbol and increases the height of the symbol after the ball has been successfully returned to the opposite side of the net two times in succession.

2-112. Just prior to each serve, the SERVE signal goes high, which clears counter K2. With the outputs at pins 9, 8, and 11 of counter K2 low, a BCD 0001 is loaded into counter K3 when the 128V signal goes low (top half of picture). When the 128V signal goes high, K3 starts counting 4V pulses. While K3 is counting, pin 15 of K3 is low, which forces the output of NAND gate K4-8 to be high. The output of NAND gate H2-8 is also high at this time, which forces the output of gate K4-6 low. Consequently, flip-flop B2-8 is held in a preset state (pin B2-8 low), which inhibits NAND gate B8-12.

2-113. When K3 reaches its terminal count, pin K3-15 goes high. Providing the lower half of the TV screen (indicated when signal 128V is high) is being swept by the electron beam, the output of NAND gate K4-8 goes low, which stops counter K3 and forces the output of gate K4-6 high. Thus, the next time a positive-going 2H pulse occurs when the 256H signal is low (left half of picture), the Q output of flip-flop B2-8 is clocked high. When the 256H signal goes high at the approximate vertical center of the picture, NAND gate B8-12 has enabling levels at pins 1 and 13. Therefore, each time the 4V signal goes high, a low NET signal is developed that causes another portion of the net symbol to appear on the TV screen. In addition, the low NET HEIGHT signal taken from the output of inverter B5-10 is sent to the out-of-bounds/fourth hit/net hit circuit to indicate the presence of the net symbol. This process continues until time 256V.

2-114. After 256V, counter K3 is preset by a low 128V signal and the outputs of NAND gates H2-8 and K4-8 go high. Flip-flop B2-8 is preset by the low output of gate K4-8, which inhibits gate B8-12 and establishes the bottom of the net. As a result, a net symbol that consists of a series of short vertical lines is formed on the TV screen.

2-115. After the ball is served, the SERVE signal goes high. If the ball is returned, the BALL MOTION signal goes high momentarily. One-shot K1-9 is triggered by the high SERVE signal and positive-going BALL MOTION pulse and produces a negative-going pulse at the $\overline{Q}$ output, which is applied to flip-flop J1-5/6. Assuming this flip-flop is in a cleared state, the trailing edge negative-going pulse clocks the Q output to a high level. The next positive-going BALL RETURN pulse causes the Q output of flip-flop J1-5/6 to be clocked to a low level, which causes counter K2 to be augmented by one count. If the ball continues in play, the counter is augmented once for every two times the ball is returned. Each time the 128V signal goes low, counter K3 is preset to a new count that is determined by the current count contained in counter K2. When the 128V signal goes high, counter K3 begins counting from the preset value. Thus, as the count builds in counter K2, the time required for counter K3 to reach its terminal count decreases. Con-

sequently, the net symbol is allowed to appear earlier after every two returns of the ball. This process continues until counter K2 reaches the BCD count of 0101 (decimal 10). At this point, the low output of NAND gate H1-6 holds flip-flop J1-5/6 in a cleared state, which prevents counter K2 from being augmented and, therefore, the net from increasing in height. Counter K2 is reset after the next serve, and the net is accordingly reduced to its minimum height.

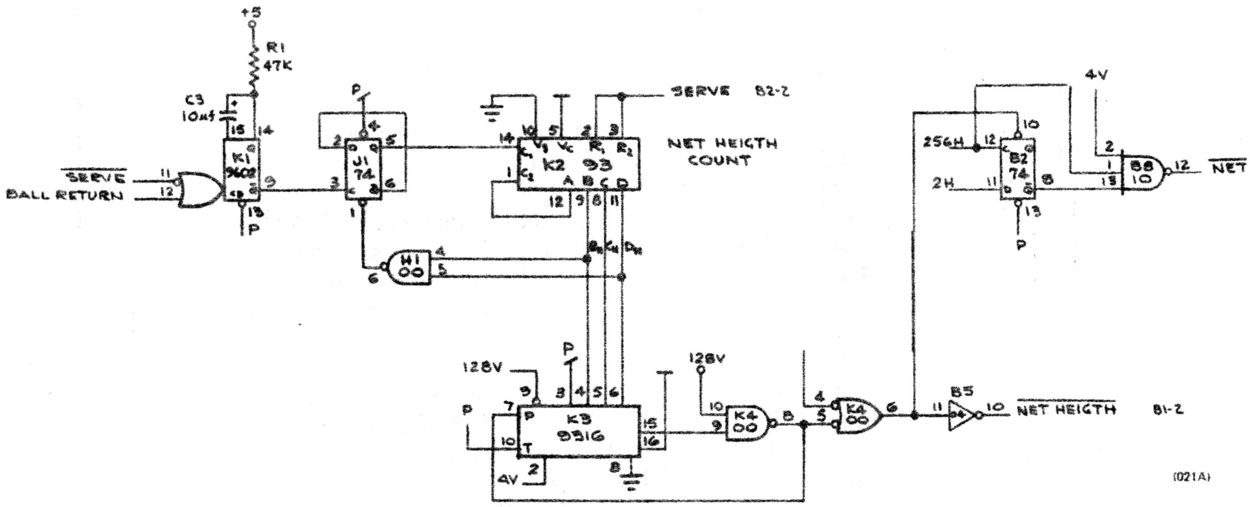


Figure 2-19. Net Circuit

Table 2-1. Rebound PCB Parts List

ITEM	PART NO.	QTY.	DESCRIPTION
1	10101	3	100 ohm ± 10%, 1/4 W, Resistor
2	10102	9	1 K ohm " " "
3	10104	3	100 K ohm " " "
4	10151	1	150 ohm " " "
5	10221	1	220 ohm " " "
6	10331	7	330 ohm " " "
7	10333	1	33 K ohm " " "
8	10470	2	47 ohm " " "
9	10473	3	47 K ohm " " "
10	19100	1	4 ohm ± 20%, 10W, Resistor, Wirewound
11	30100	1	100 pf Capacitor, Mica
12	30102	2	220 " " "
13	32101	1	0.1 uf Capacitor Mylar, ± 10%, 6V
14	34101	17	0.1 uf Ceramic Bypass Capacitor
15	35103	2	10 uf Capacitor, Electrolytic, 6V
16	35254	1	250 uf Capacitor Electrolytic, 6V
17	35473	2	47 " " " "
18	35502	1	5.0 " " " 10V
19	37000	1	8000 uf Capacitor Electrolytic, 16V
20	60000	2	Switch, DPDT Slide, PC Mount
21	70000	2	2N3643 Transistor
22	70001	1	2N3644 "
23	71000	4	1N914 Diode
24	71001	1	4001 Diode
25	71006	2	Diode, GE No. A14u
26	72000	8	7400 Integrated Circuit
27	72001	4	7402 " "
28	72002	3	7404 " "
29	72003	7	7410 " "
30	72004	1	7420 " "
31	72006	1	7427 " "
32	72007	1	7430 " "
33	72008	1	7448 " "
34	72009	1	7450 " "
35	72010	11	7474 " "
36	72011	1	7483 " "
37	72012	2	7486 " "
38	72013	2	7490 " "
39	72014	6	7493 " "
40	72015	4	74107 " "
41	72016	2	74153 " "
42	72017	8	9316 " "
43	72018	3	555 " "
44	72019	1	LM309K Voltage Regulator
45	72025	1	9322 Integrated Circuit
46	72026	2	9602 " "
47	72027	3	7408 " "
48	72035	1	74193 " "
49	75100	2	Screw, No. 6-32x5/8 Stainless St. Pan Hd.
50	75101	4	Washer, Lock No. 6-32 Internal Star, Stainless
51	75102	2	Washer, No. 6-32 Flat
52	75103	2	Hex Nut, No. 6-32
53	81001	1	Crystal, 14.31818 mhz
54	83014	1	Heatsink, Wakefield No. 690-3-B
55	84001	A/R	Heatsink Compound, Dow No. 340
56	000517	1	PCB Rev. C
57	000795	Ref	Schematic Rev. C
58	G000846	Ref	Artwork Rev. C

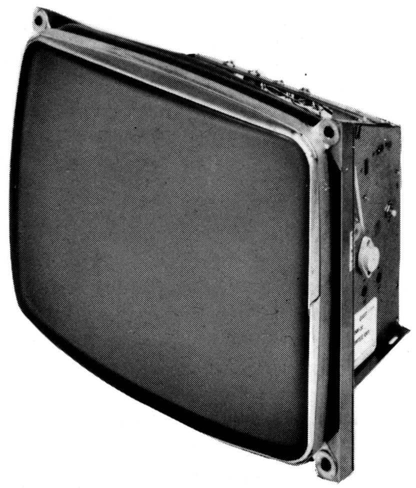
MOTOROLA service manual

FILE VP11

VISUAL
DISPLAY PRODUCTS

CHASSIS
19VP102
C19VP102
23VP102

MODEL
XM500-10
XM500-11
XM700-10



GENERAL INFORMATION

These models are transistorized monitors designed for the video game market.

The chassis permits incorporation of optional operating control locations and provides support for the CRT.

Circuitry includes four stages of video amplification, a two stage audio amplifier, sync and deflection circuits and a regulated power supply. An additional 5 volt 1.5 amp supply is included to power external logic systems. The picture tube is a 110 degree deflection CRT with implosion protection. Composite video is fed to the monitor through a connector mounted on the rear of the chassis.

Rear panel controls include Horizontal Hold, Vertical Hold, Contrast, Brightness and Volume. The width control (on some models) is mounted on a bracket at the rear of the chassis. Additional service controls are mounted on the plated circuit panel, and are accessible from the rear of the chassis.

The chassis utilizes plug-in etched panel construction with components mounted on the top side and plated wiring on the bottom. Component reference numbers and circuit legend are printed on the board to aid in servicing. Horizontal, vertical output and regulator transistors plus regulator IC are mounted on two vertical side brackets which serve as a heat sink and CRT support.

ELECTRICAL SPECIFICATIONS

Power Rating: 80 watts nominal.

Source: 120/240V AC at 50/60 cycles.

Video Input: 0.5 to 2.5 volts composite PP (sync negative).

Audio Output: 5 watts peak.

CAUTION

NO WORK SHOULD BE ATTEMPTED ON ANY EXPOSED MONITOR CHASSIS BY ANYONE NOT FAMILIAR WITH SERVICING PROCEDURES AND PRECAUTIONS.

MODEL BREAKDOWN CHART

MODEL	CHASSIS	LINE VOLTAGE & FREQ	CRT	INPUT IMPEDANCE
XM500-10	19VP102	Wired for 120V AC 60 cycle	See V1 in Replacement Parts List	–
XM500-11	C19VP102	Switch selected 120/240V AC at 50/60 cycles		1.5K
XM700-10	23VP102			470 Ω

TABLE OF CONTENTS

MOTOROLA INC. **Consumer Products Division** FRANKLIN PARK, ILLINOIS 60131

PART NO. 68P65130A66 1-74 PRICE $1.00

SAFETY WARNING

CAUTION: NO WORK SHOULD BE ATTEMPTED ON AN EXPOSED MONITOR CHASSIS BY ANYONE NOT FAMILIAR WITH SERVICING PROCEDURES AND PRECAUTIONS.

1. SAFETY PROCEDURES should be developed by habit so that when the technician is rushed with repair work, he automatically takes precautions.

2. A GOOD PRACTICE, when working on any unit, is to first ground the chassis and to use only one hand when testing circuitry. This will avoid the possibility of carelessly putting one hand on chassis or ground and the other on an electrical connection which could cause a severe electrical shock.

3. Extreme care should be used in HANDLING THE PICTURE TUBE as rough handling may cause it to implode due to atmospheric pressure (14.7 lbs. per sq. in). Do not nick or scratch glass or subject it to any undue pressure in removal or installation. When handling, safety goggles and heavy gloves should be worn for protection. Discharge picture tube by shorting the anode connection to chassis ground (not cabinet or other mounting parts). When discharging, go from ground to anode or use a well insulated piece of wire. When servicing or repairing the monitor, if the cathode ray tube is replaced by a type of tube other than that specified under the Motorola Part Number as original equipment in this Service Manual, then avoid prolonged exposure at close range to unshielded areas of the cathode ray tube. Possible danger of personal injury from unnecessary exposure to X-ray radiation may result.

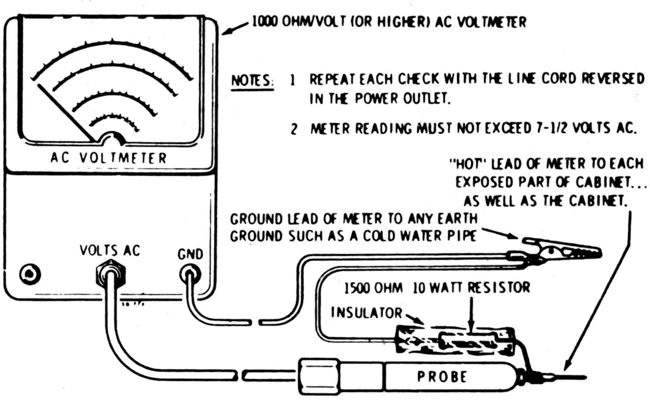
4. An ISOLATION TRANSFORMER should always be used during the servicing of a unit whose chassis is connected to one side of the power line. Use a transformer of adequate power rating as this protects the serviceman from accidents resulting in personal injury from electrical shocks. It will also protect the chassis and its components from being damaged by accidental shorts of the circuitry that may be inadvertently introduced during the service operation.

5. Always REPLACE PROTECTIVE DEVICES, such as fishpaper, isolation resistors and capacitors and shields after working on the unit.

6. If the HIGH VOLTAGE is adjustable, it should always be ADJUSTED to the level recommended by the manufacturer. If the voltage is increased above the normal setting, exposure to unnecessary X-ray radiation could result. High voltage can accurately be measured with a high voltage meter connected from the anode lead to chassis.

7. BEFORE RETURNING A SERVICED UNIT, the service technician must thoroughly test the unit to be certain that it is completely safe to operate without danger of electrical shock. DO NOT USE A LINE ISOLATION TRANSFORMER WHEN MAKING THIS TEST.

In addition to practicing the basic and fundamental electrical safety rules, the following test, which is related to the minimum safety requirements of the Underwriters Laboratories should be performed by the service technician before any unit which has been serviced is returned.



Voltmeter Hook-up for Safety Check.

A 1000 ohm per volt AC voltmeter is prepared by shunting it with a 1500 ohm, 10 watt resistor. The safety test is made by contacting one meter probe to any portion of the unit exposed to the operator such as the cabinet trim, hardware, controls, knobs, etc., while the other probe is held in contact with a good "earth" ground such as a cold water pipe.

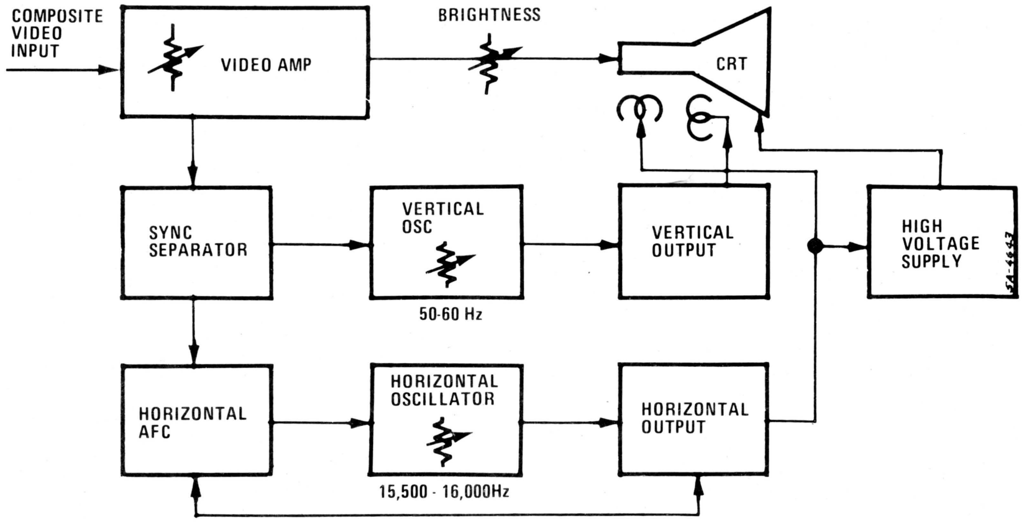
The AC voltage indicated by the meter may not exceed 7½ volts. A reading exceeding 7½ volts indicates that a potentially dangerous leakage path exists between the exposed portion of the unit and "earth" ground. Such a unit represents a potentially serious shock hazard to the operator.

The above test should be repeated with the power plug reversed, when applicable.

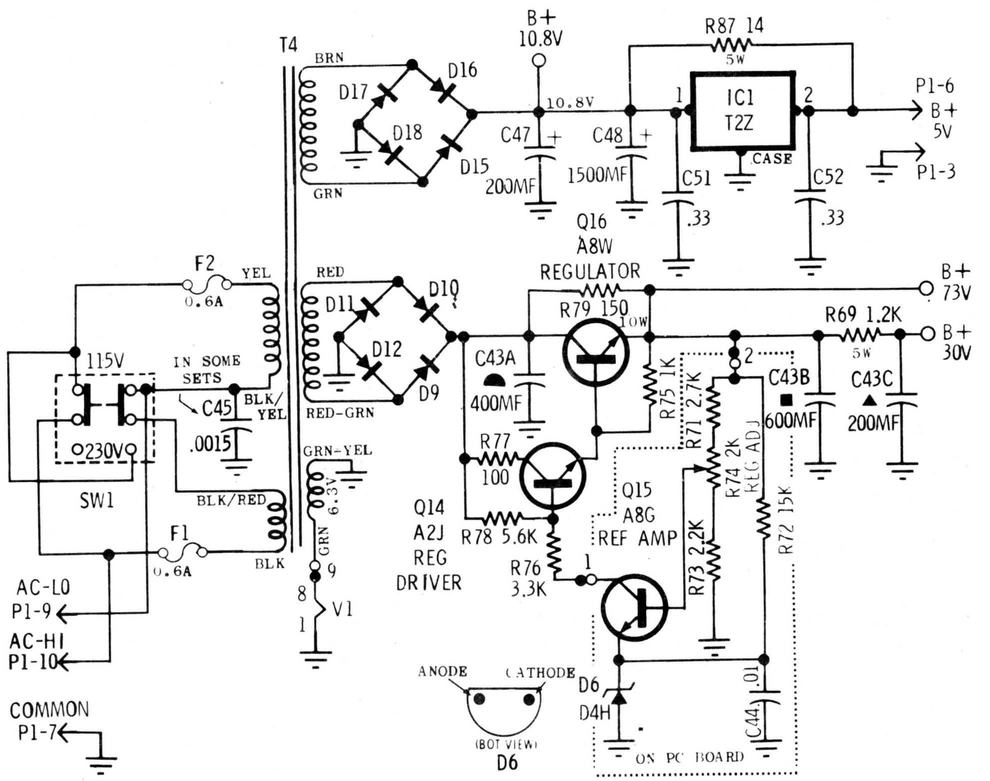
NEVER RETURN A MONITOR which does not pass the safety test until the fault has been located and corrected.

THEORY OF OPERATION

CRT DISPLAY MODULE - COMPOSITE VIDEO SYSTEM



Block Diagram



POWER SUPPLY

The power supply is a transformer operated, full wave, regulated supply which maintains constant output voltage with input variations of ± 15%. A switch (SW1) is provided to allow operation from 115/230 volts, 50/60Hz. The regulator is a series pass circuit. Q16 is the series pass transistor, Q15 the reference amplifier and Q14 the output driver.

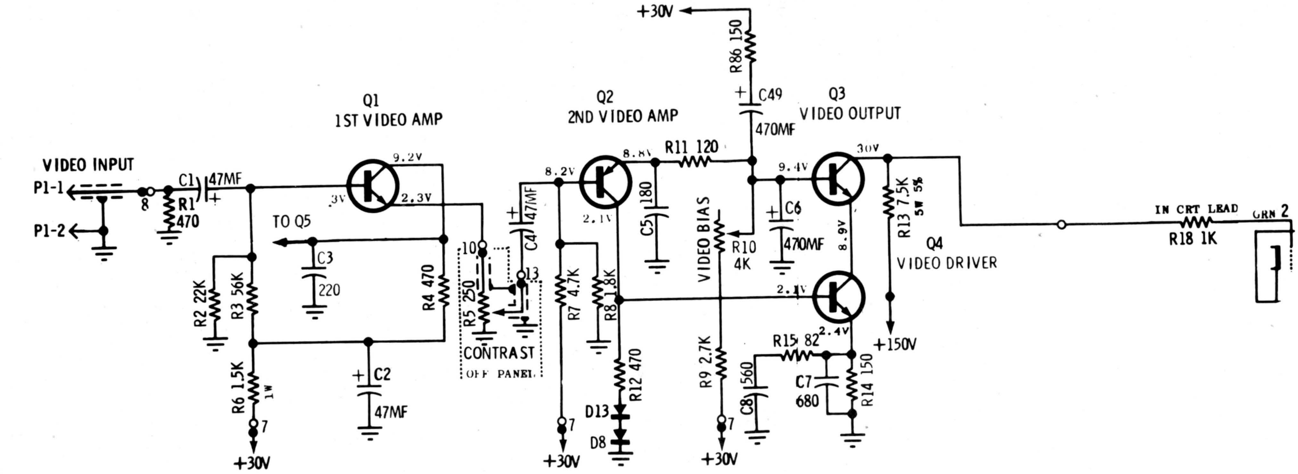
The output voltage of the regulator appears at the emitter of Q16. This voltage is divided between R71, R74 and R73. The voltage appearing on the arm of potentiometer R74 is a reference input to the base of Q15.

A temperature compensated zener diode (D6) is used to establish a fixed reference voltage at the emitter of Q15. R72 provides a bias current for D6, establishing its operating point.

An increase in output voltage will result in an increase of voltage at the base of Q15. Since the emitter of Q15 is held at a fixed reference voltage, the change in base voltage will turn Q15 on harder, reducing its collector voltage. This reduces forward bias for Q14 resulting in less emitter current and less base current for Q16. Q16 will conduct less, lowering the output voltage.

R79 provides a shunt current path for Q16 allowing it to run cooler, improving reliability. C44 is an RF noise filter.

A regulated 1.5 amp, 5V DC supply is used to power circuits external from the monitor. Its operation is similar to the 73V regulator except all of the circuitry is contained in one IC package.



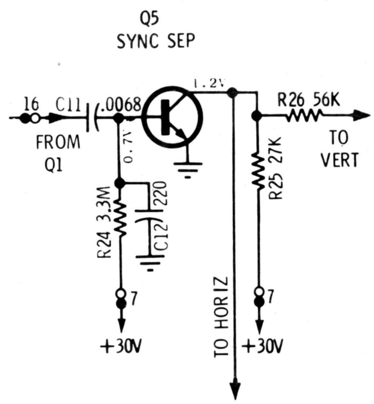
VIDEO AMPLIFIER

The video amplifier has four stages incorporating devices Q1, Q2, Q3 and Q4. The first stage, Q1, functions as an emitter follower. The low output impedance of the first stage permits use of a low resistance contrast control which furnishes flat video response over its entire range without the need for compensation. The collector output of Q1 is used to drive the sync separator. C3 provides high frequency roll off to limit the collector output to the bandwidth required to pass synchronization signals. Q2 is a common emitter stage and is directly coupled to Q4. Q3 and Q4 are connected in a cascode configuration. This common emitter-common base connection greatly reduces the effect of Miller capacity compared with a conventional single transistor video output stage. C6 provides a ground for video at the base of Q3, the grounded base transistor of the video output cascode pair. Diodes D13 and D8 provide temperature compensation for the video output stages.

The video bias control R10, is used to set the quiescent collector voltage of Q3. C5, C7, C8 and R15 are used for high frequency compensation. The video amplifier output is direct coupled to the control grid of the CRT through R18 which is used to isolate Q3 from transients that may occur as a result of CRT arcing.

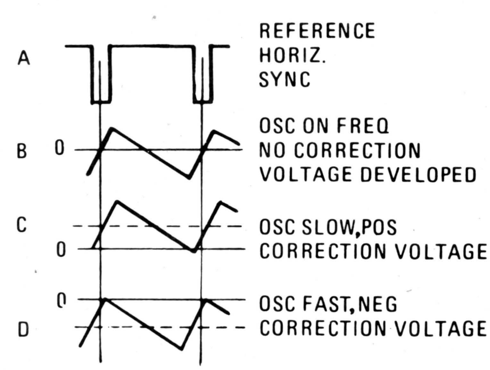
SYNC SEPARATOR

The sync separator employs a single stage, Q5, to recover sync from the composite video signal. A single stage sync separator is adequate due to the high impedance of the following stages. The video input to the sync separator is black positive. C11 is charged by the peak base current that flows when the positive peak of the input takes Q5 to saturation. This charge depends on the peak to peak input to Q5 and thus makes the bias for Q5 track the amplitude of the input signal. As a result Q5 amplifies only the positive peaks of the input signal. The initial bias current through R24 sets the clipping level.



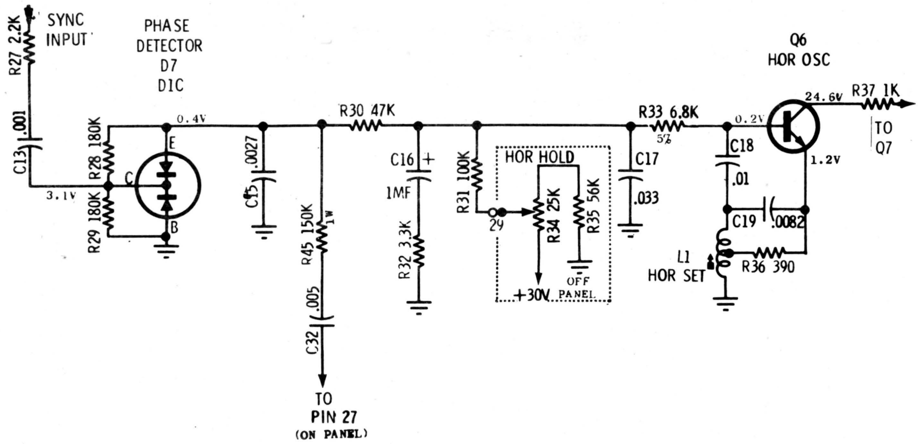
PHASE DETECTOR

The Phase Detector consists of two diodes in a keyed clamp circuit. Two inputs are required to generate the required output, one from the sync separator and one from the horizontal deflection system. The required output must be of the correct polarity and amplitude to correct phase differences between the input sync and the horizontal time base. The horizontal collector pulse is integrated into a sawtooth by R45 and C15. During sync time both diodes in D7 conduct, shorting C15 to ground.



The sawtooth on C15 is thus clamped to ground at sync time. If the horizontal time base is in phase with the sync, the sync pulse will occur when the sawtooth is passing through its AC axis and the net charge on C15 will be zero. (Figure B). If the horizontal time base is lagging the sync, the sawtooth on C15 will be clamped to ground at a point negative from the AC axis. This will result in a positive DC charge on C15. (Figure C). This is the correct polarity to cause the horizontal oscillator to speed up to correct the phase lag.

Likewise, if the horizontal time base is leading the sync, the sawtooth on C15 will be clamped at a point positive from its AC axis, resulting in a net negative charge on C15 which is the required polarity to slow the horizontal oscillator (Figure D). R30, C17, C16 and R32 comprise the phase detector filter. The bandpass of this filter is chosen to provide correction of horizontal oscillator phase without ringing or hunting.

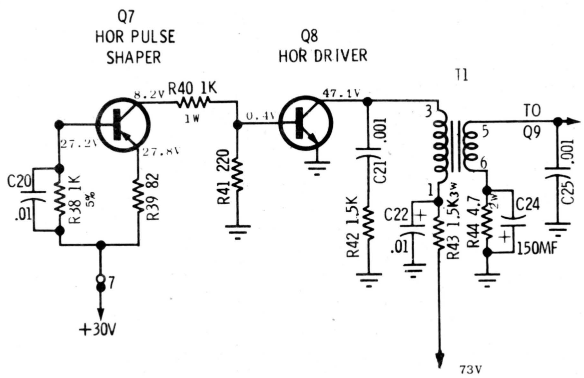


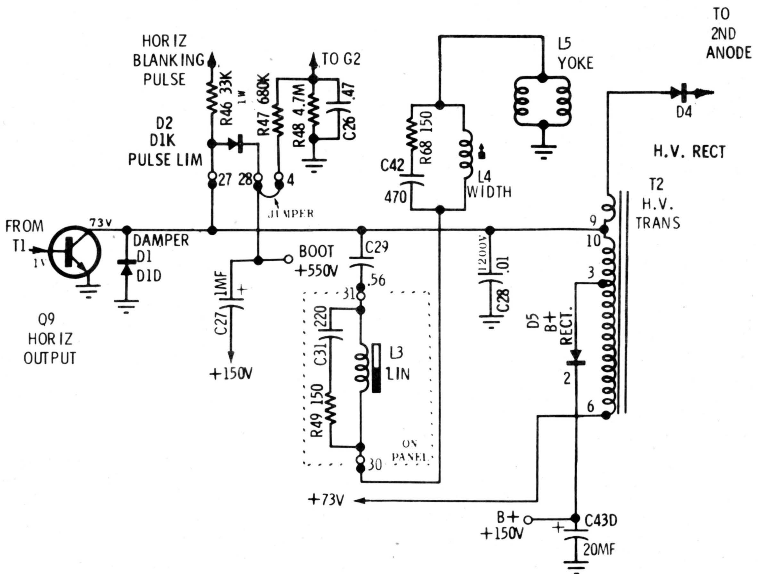
HORIZONTAL OSCILLATOR

Q6 is employed in a modified type of Hartley oscillator. The operating frequency of this oscillator is sensitive to its base input voltage. This permits control by the output of the phase detector and also by the setting of the horizontal hold control, R34. The horizontal hold range is set by adjustment of the core of L1.

PULSE SHAPER & HORIZONTAL DRIVER

Q7 is used as a buffer stage between the horizontal oscillator and the horizontal driver. It provides isolation for the horizontal oscillator as well as a low impedance drive for the horizontal driver. R38 and C20 form a time constant which shapes the oscillator output to the required duty cycle (approximately 50%), to drive the horizontal output circuitry. The horizontal driver stage, Q8 operates as a switch to drive the horizontal output transistor through T1. Because of the low impedance drive and fast switching times furnished by Q7, very little power is dissipated in Q8. C21 and R42 provide damping to suppress ringing of the primary of T2 when Q8 goes into cutoff.

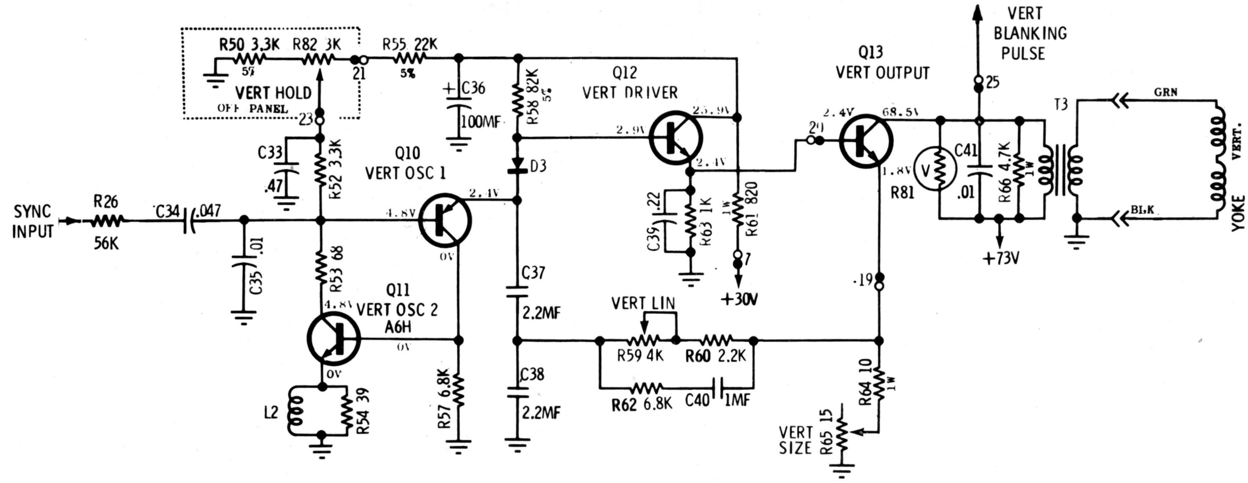




HORIZONTAL OUTPUT

The secondary of T1 provides the required low drive impedance for Q9. R44 and C24 form a time constant for fast turn-off of the base of Q9. Q9 operates as a switch which, once each horizontal period, connects the supply voltage across the parallel combination of the horizontal deflection yoke and the primary of T2. The required sawtooth of deflection current through the horizontal yoke is formed by the L-R time constant of the yoke and output transformer primary. The horizontal retrace pulse charges C27 through D2 to provide operating voltage for G2 of the CRT. Momentary transients at the collector of Q9, should they occur, are limited to the voltage on C27 since D2 will conduct if the collector voltage exceeds this value.

The damper diode, D1, conducts during the period between retrace and turn on of Q9. C28 is the retrace tuning capacitor. C29 blocks DC from the deflection yoke. L3 is a magnetically biased linearity coil which shapes deflection current for optimum trace linearity. L4 is a series width control. C31 and R49, C42 and R68 are damping network components for the linearity and width controls. C43D is charged through D5 developing the video supply voltage.

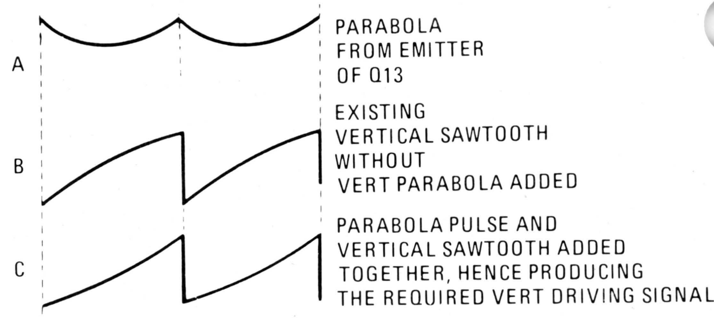


VERTICAL OSCILLATOR DRIVER AND OUTPUT

Sync from the collector of Q5 is integrated by R26 and C35. Q10 and Q11 are connected as a regenerative switch. The series combination of C37 and C38 charges through R58 and D3 until Q10 turns on. This occurs when the emitter of Q10 exceeds its base voltage and causes current to flow into the base of Q11, turning that device on. When Q10 and Q11 conduct, C37 and C38 are discharged to nearly zero. Q10 and Q11 then shut off and the cycle repeats. The setting of R82 determines the repetition rate of the charge and discharge of C37 and C38. The waveform generated is a positive going ramp or sawtooth with a fast retrace to zero. D3 provides a small incremental voltage above ground to overcome the forward base-emitter drop of the two following stages. Q12 is an emitter follower used to transform the high impedance drive sawtooth to a low impedance drive for Q13.

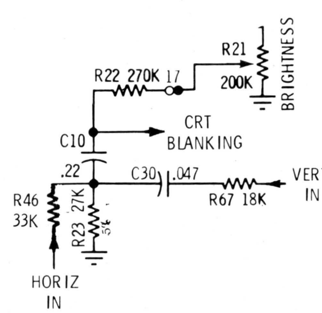
T3 matches the collector of Q13 to the vertical yoke. When Q13 is cut off during vertical retrace, a high voltage pulse is developed across the primary of T3. To limit this pulse to a safe value a varistor, R81, is connected across the primary. R66 and C41 provide damping to shape the collector pulse so it may be used for retrace blanking. Since the primary impedance of T3 decreases with current, the degree to which the primary shunts the reflected load impedance varies with collector current. This would result in severe vertical non-linearity unless some compensation is employed.

Resistors R59 and R60 couple the emitter voltage of Q13 to the junction of C37 and C38. Since this path is resistive, the waveform coupled back will be integrated into a parabola by C38. This results in a pre-distortion of the drive sawtooth as shown in Figure C. This is done to compensate for the non linear charging of C37 and C38 and the changing impedance of the primary of T3. An additional feedback path through R62 and C40 serves to optimize the drive waveshape for best linearity.



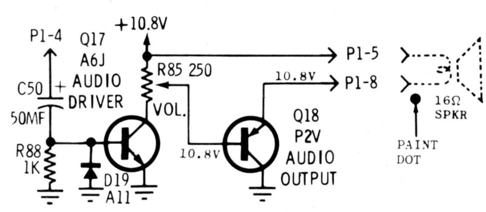
RETRACE BLANKING

Both vertical and horizontal retrace blanking are provided by positive pulses applied to the CRT cathode. The collector pulse from the horizontal output transistor is placed across R23 through R46. The vertical collector voltage is differentiated by C30 to remove the sawtooth portion of the waveform. The remaining pulse appears across R23. The mixed vertical and horizontal pulses on R23 are coupled to the CRT cathode by C10.



AUDIO AMPLIFIER

Q17 and Q18 form a DC coupled "switching tone burst amplifier". An input signal biases Q17 on, in turn driving Q18 into conduction. When the signal is removed both stages return to a quiescent mode. Coupling capacitor C50, diode D19 and resistor R88 establish a bias voltage which is signal dependent. Volume control R85 sets the peak to peak level for the output stage.



ETCHED BOARD CIRCUIT TRACING

Component reference numbers are printed on top and bottom of the plug-in circuit board to facilitate circuit tracing. In addition, control names and board terminal numbers are also shown and are referenced on the chassis schematic diagram in this manual.

Transistor elements are identified as follows: E – emitter, B – base, and C – collector.

COMPONENT REMOVAL

Removing components from the etched board is facilitated by the fact that the circuitry (plating) appears on one side of the board only and the component leads are inserted straight through the holes and are not bent or crimped.

It is recommended that a solder extracting gun be used to aid in component removal. An iron with a temperature controlled heating element would be desirable since it would reduce the possibility of damaging the board due to over-heating.

The nozzle of the soldering gun is inserted directly over the component lead and when sufficiently heated, the solder is drawn away leaving the lead free from the copper plating. This method is particularly suitable in removing multi-terminal components.

NOTE: Misadjustment of the low voltage regulator, or the horizontal oscillator may result in damage to the Horizontal Output Transistor or pulse limiter diode. The following procedures are recommended to insure reliable operation.

REGULATOR ADJUSTMENT

1. Connect monitor to AC line supply. Adjust supply to 120 volts (240 on some models).

2. Apply test signal to proper input. Signal should be of same amplitude and sync rate as when monitor is in service.

3. Adjust vertical and horizontal oscillator controls until display is synced.

4. Connect a DC digital voltmeter or other precision accuracy voltmeter to the emitter of the regulator output transistor, (or any 73 volt test point).

5. Adjust the regulator control R74, on circuit board for an output of 73 volts. **Do not "run" the regulator control through its range or damage to the monitor may result.**

6. When adjustment is complete, the AC line supply can be varied between 105 and 130 volts to check for proper regulator operation. With regulator operating properly, changes in display size should be negligible.

HORIZONTAL OSCILLATOR ADJUSTMENT

1. Set the horizontal hold potentiometer to mid-range (R34).

2. Adjust core of horizontal hold coil L1 until the horizontal blanking lines are vertical.

3. Rotate potentiometer R34 through its full range. Display should go out of sync in each direction and hold in sync at the center of its range. Retouch L1 as necessary to center the hold range.

VIDEO AMPLIFIER BIAS ADJUSTMENT

Adjust video bias control R10 for 30 volts DC on collector of video output transistor Q3 with no signal input.

Disconnect cable from video input jack if necessary to eliminate noise.

POWER TRANSISTOR REPLACEMENT

When replacing any "plug-in" transistor, i.e., the horizontal or vertical output, please observe the following precautions:

1. The transistor sockets are not "Captive", that is, the transistor mounting screws also secure the socket. When installing the transistor, the socket must be held in its proper location. This location is indicated by flanges on the socket which fit into the heat sink.

2. When replacing the output transistors, silicone grease (Motorola Part No. 11M490487) should be applied evenly to both sides of the mica insulator.

3. All transistor mounting screws must be tight before applying power to the receiver. This insures proper cooling and electrical connections.

NON-COMPLIANCE WITH THESE INSTRUCTIONS CAN RESULT IN FAILURE OF THE TRANSISTOR AND/OR ITS RELATED COMPONENTS.

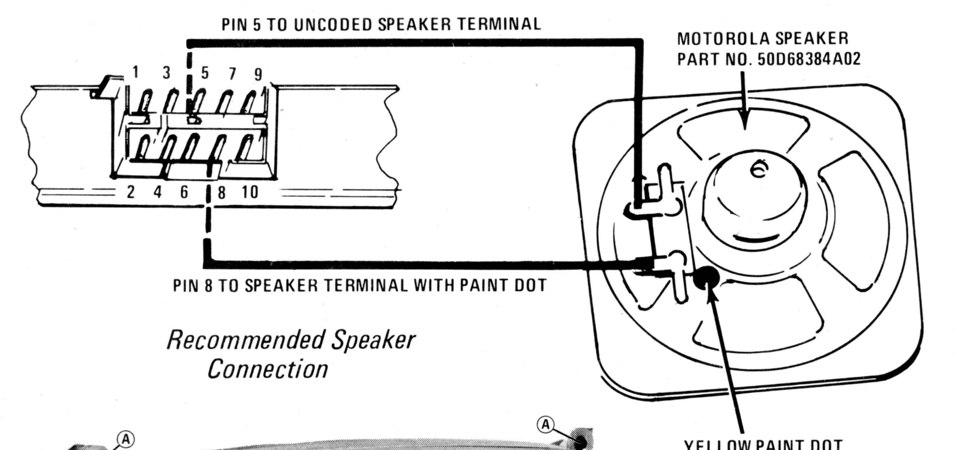
NOTE: Use caution when tightening transistor mounting screws. If the screw threads are stripped by excessive pressure, a poor electrical and mechanical connection will result.

CRT REPLACEMENT

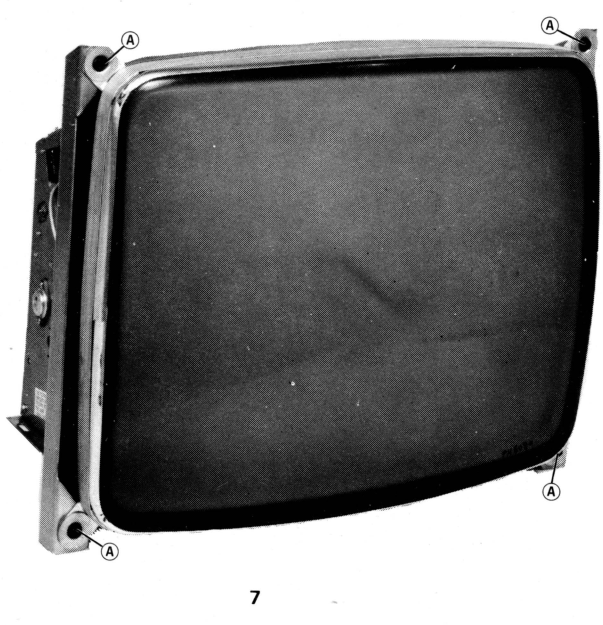
Use extreme care in handling the CRT as rough handling may cause it to implode due to atmospheric pressure. Do not nick or scratch glass or subject it to any undue pressure in removal or installation. Use goggles and heavy gloves for protection.

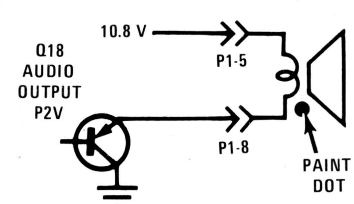
1. Discharge CRT by shorting 2nd anode to GND. Remove CRT socket, yoke and 2nd anode lead.

2. Remove CRT from chassis by removing four screws Ⓐ at corners.

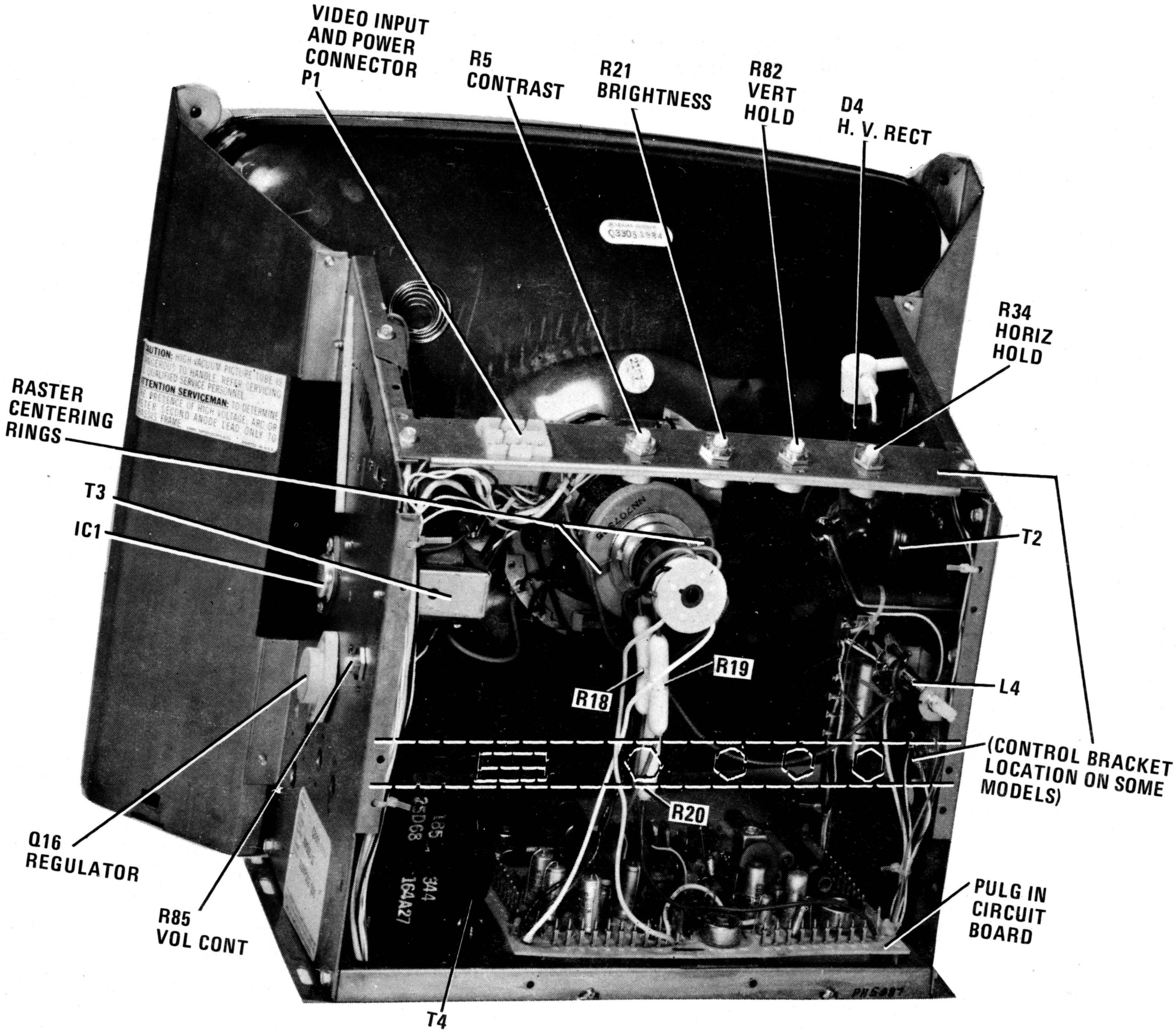


Recommended Speaker Connection

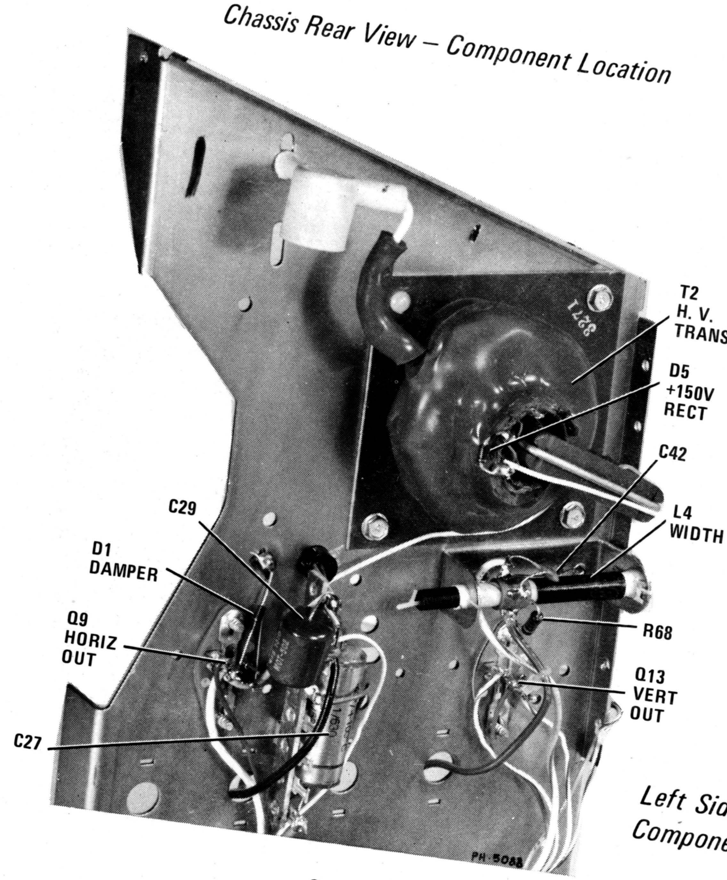




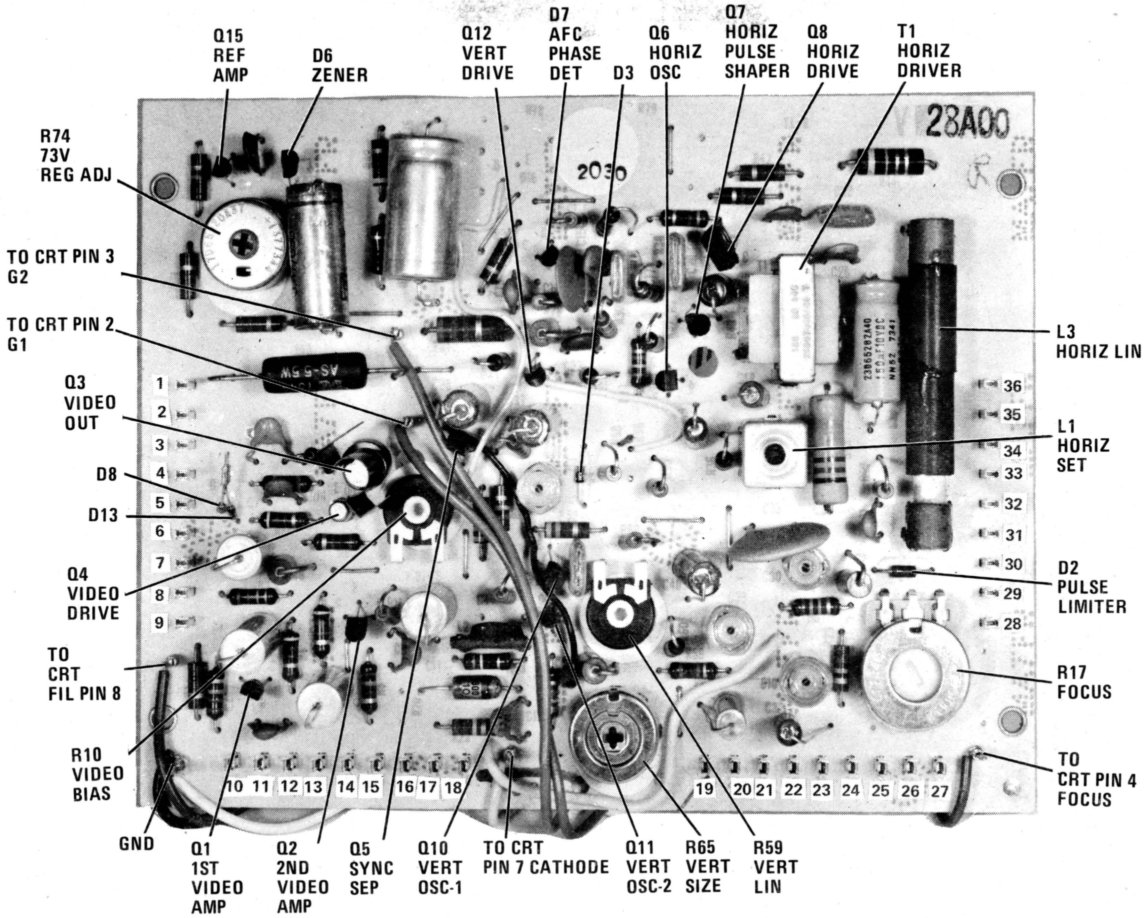
CRT Replacement



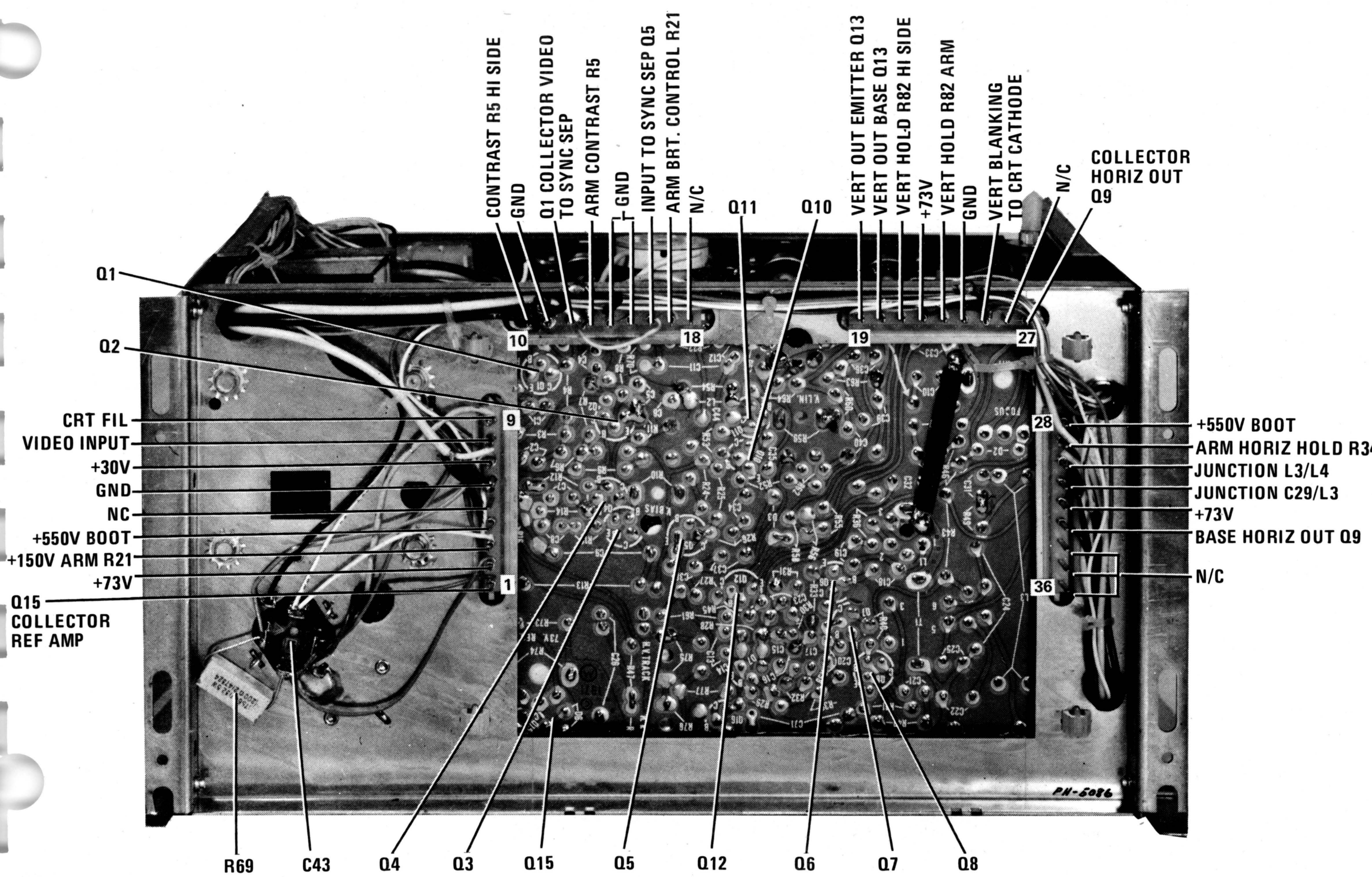
Chassis Rear View – Component Location



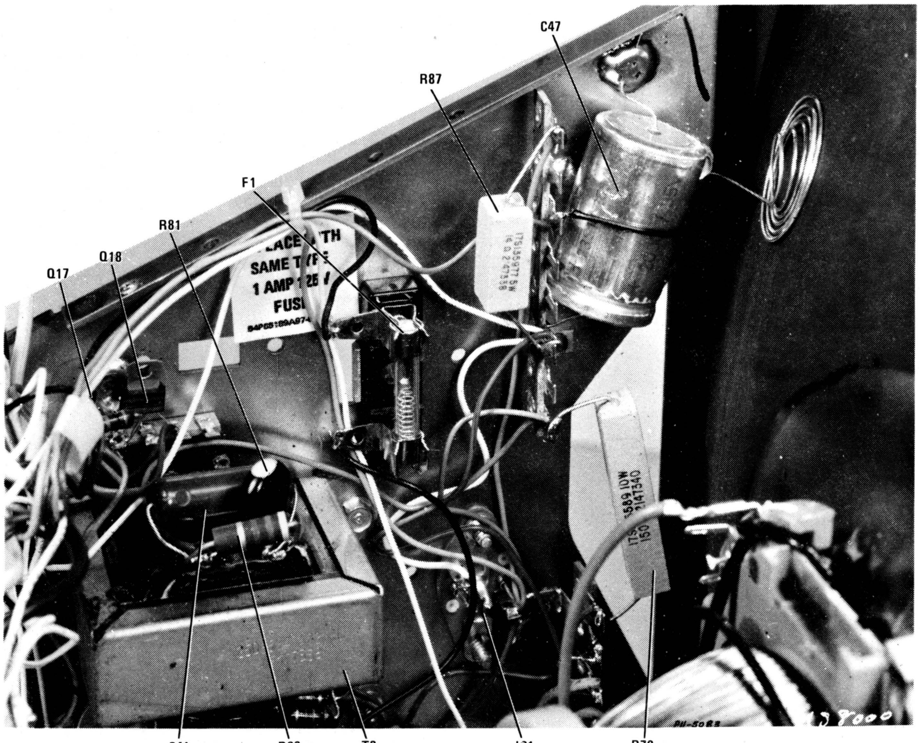
Left Side Panel – Component Location



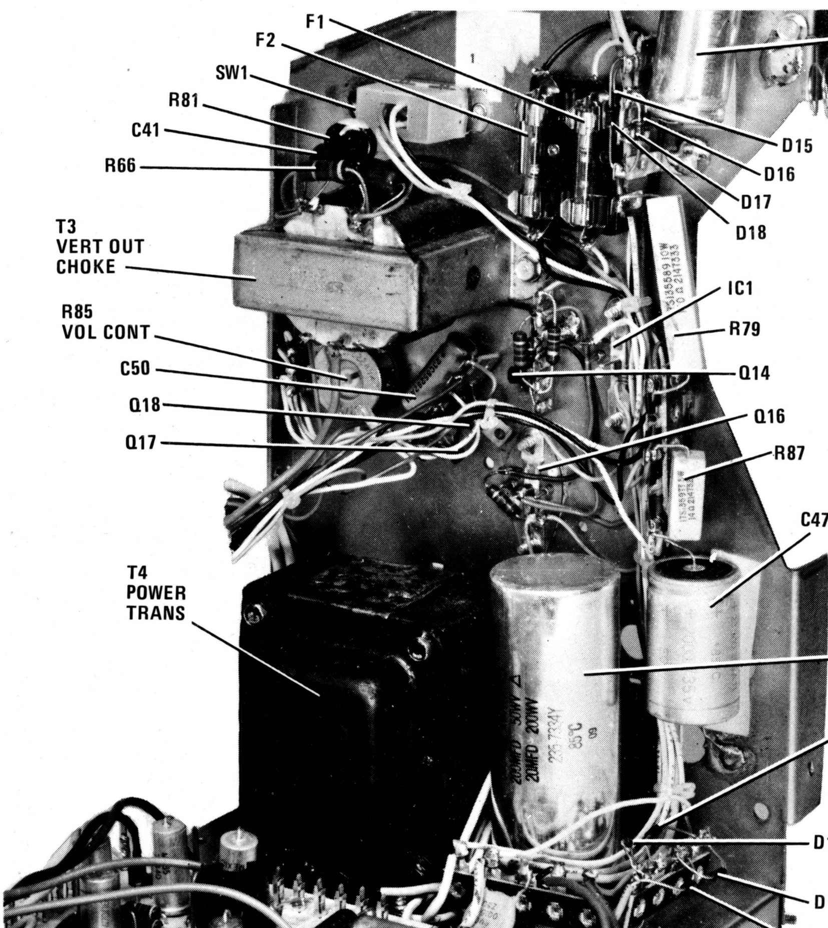
Circuit Board Top View – Component and Terminal Location



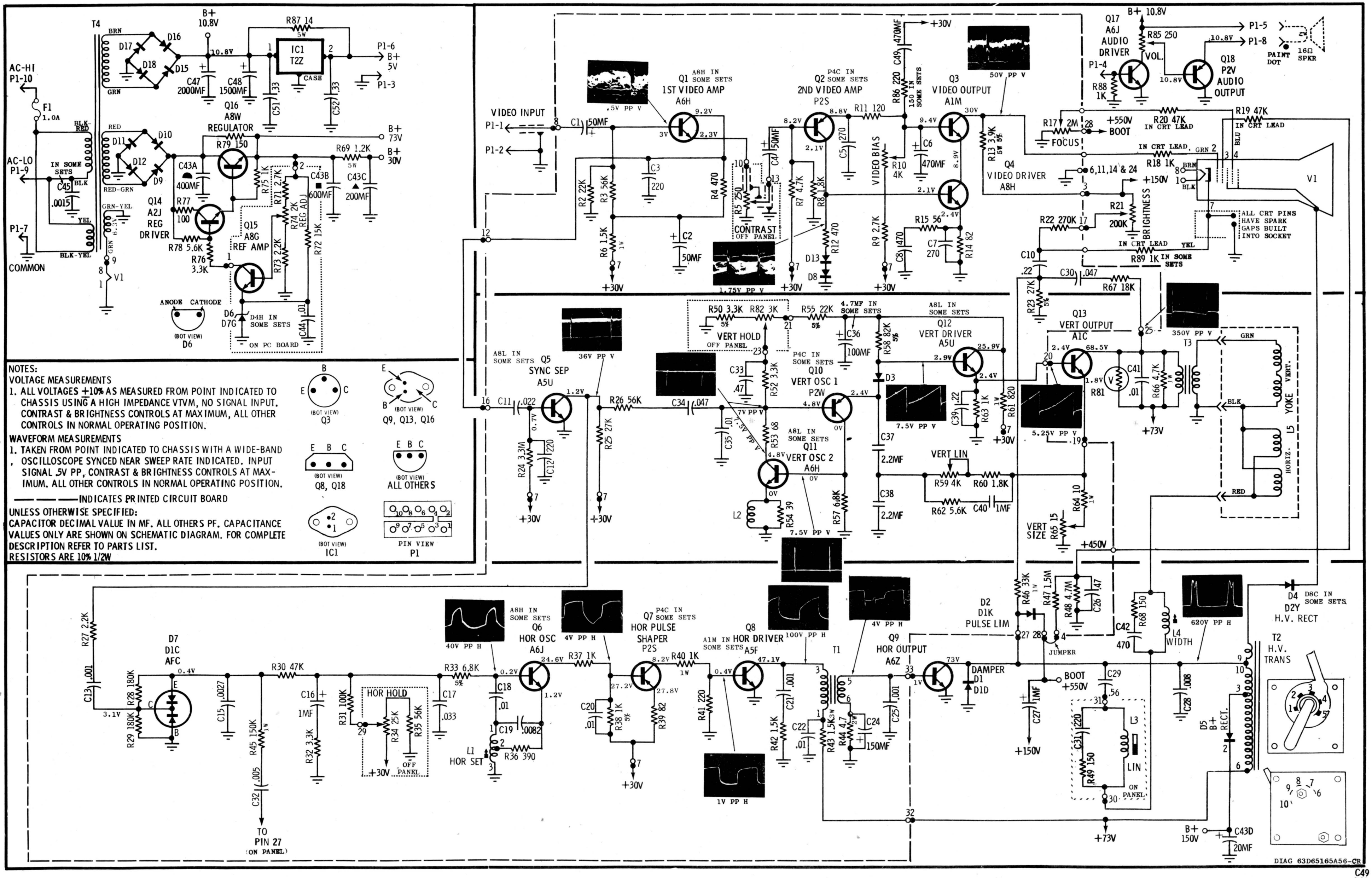
Chassis and Circuit Board Bottom View – Component and Terminal Location



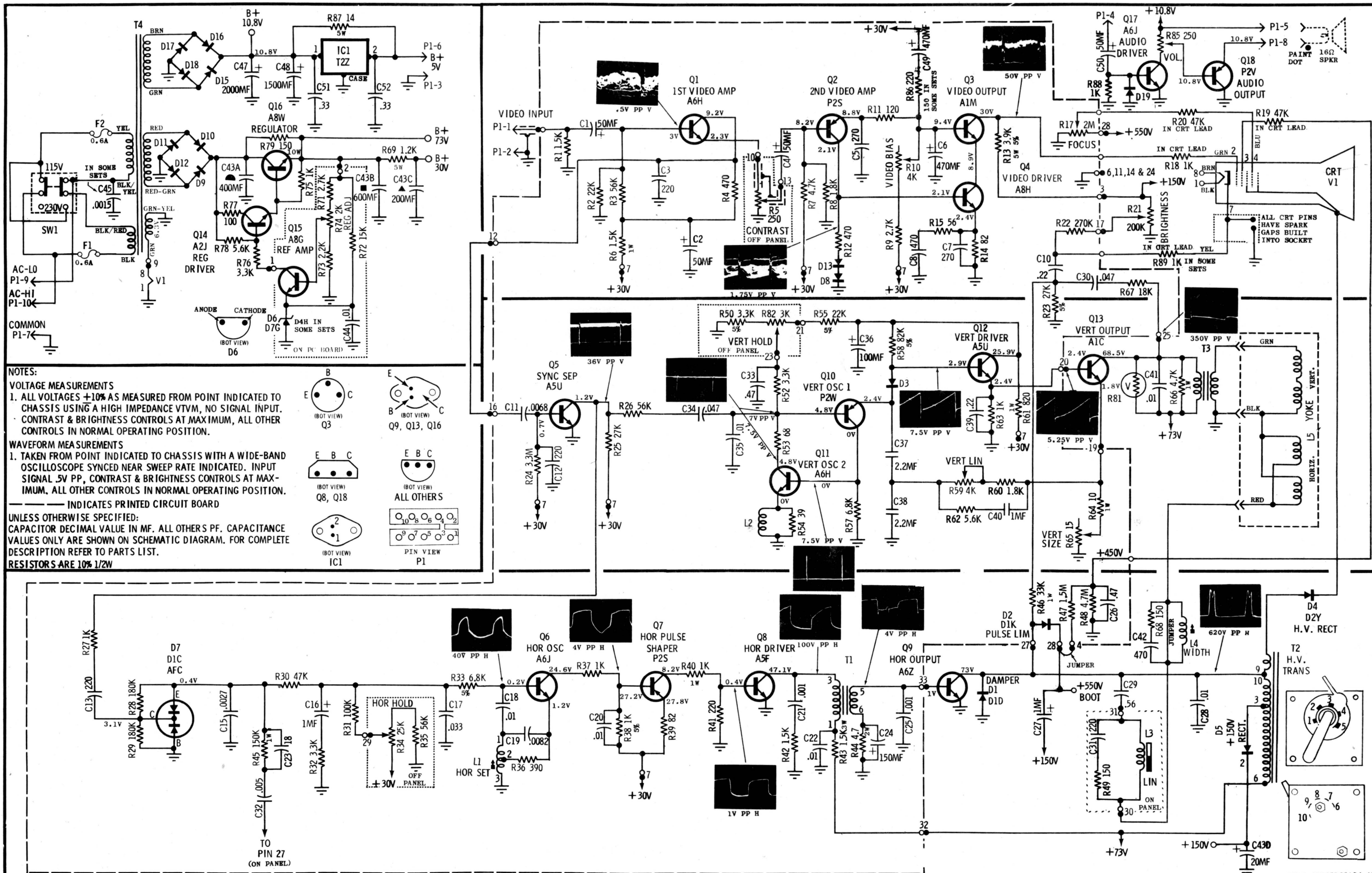
MODEL XM500-10 *Right Side Panel – Component Location*



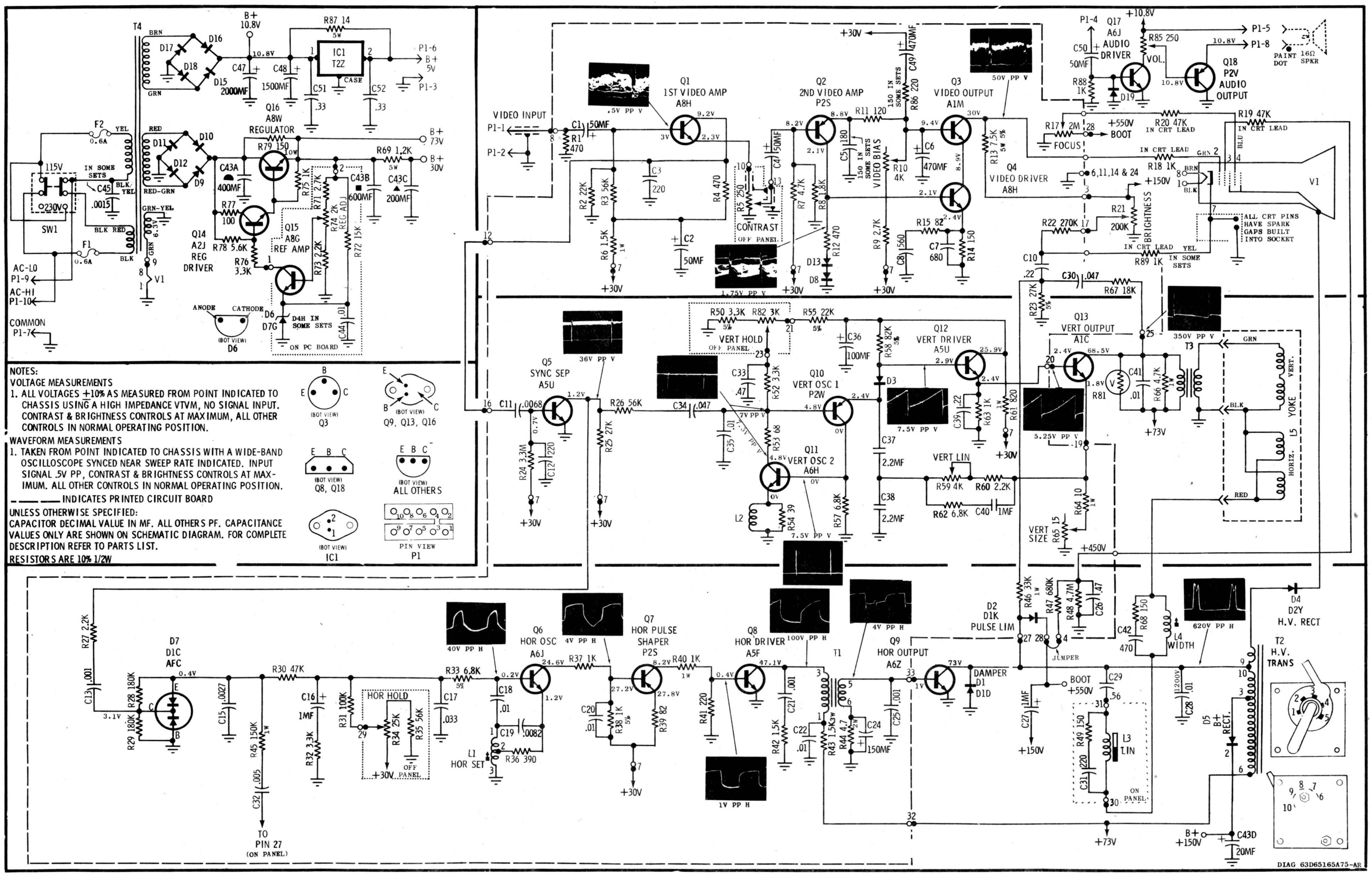
MODEL XM500-11 *Right Side Panel – Component Location*
XM700-10



Model XM500-10 Schematic Diagram



Model XM500-11 Schematic Diagram



Model XM700-10 Schematic Diagram

REPLACEMENT PARTS LIST
MODEL XM500-10-CHASSIS 19VP102

ELECTRICAL PARTS

REF. NO.	PART NUMBER	DESCRIPTION
	1Y25016A75	MONITOR PANEL: "V24A"; complete KT321KM

CAPACITORS

REF. NO.	PART NUMBER	DESCRIPTION
C1	23C65282A41	50 mf 50V Lytic
C2	23C65282A41	50 mf 50V Lytic
C3	21S180D10	220 pf 20% 100V X5F (Use 21R132503)
C4	23C65282A41	50 mf 50V Lytic
C5	21S180E78	270 pf 10% 500V X5F
C6	23S10255A78	470 mf 16V Lytic
C7	21S180E78	270 pf 10% 500V X5F
C8	21S180B53	470 pf 10% 500V X5F
C10	8S10191B67	.22 mf 10% 250V polyester
C11	8S10191A59	.022 mf 10% 100V polyester
C12	21S180D10	220 pf 20% 100V X5F (Use 21R132503)
C13	21S180B51	.001 mf 10% 500V X5F
C15	21S180C41	.0027 mf 10% 500V Z5F (Use 21K121699)
C16	23S10229A07	1.0 mf +40–20% 15V Lytic (Use 23C43280A17)
C17	8S10191B90	.033 mf 10% 160V polyester
C18	8S10299A73	.01 mf 10% 100V poly carb
C19	8S10299A74	.0082 mf 10% 160V poly carb
C20	8S10191B98	.01 mf 10% 250V polyester
C21	21S180B51	.001 mf 10% 500V X5F
C22	8S10191B98	.01 mf 10% 160V polyester
C24	23D65282A40	150 mf 10V Lytic
C25	21S180B51	.001 mf 10% 500V X5F
C26	8S10212B53	.47 mf 10% 630V mtlz poly
C27	8S10212A11	1.0 mf 10% 630V mtlz poly
C28	8S10571A05	.008 mf 5% 1200V
C29	8S10212D33	.56 mf 10% 250V mtlz poly
C30	8S10191A32	.047 mf 10% 250V polyester
C31	21S180B87	220 pf 10% 500V X5F
C32	21S180D34	.005 mf 20% 1KV Z5F (Use 21S180D31)
C33	8S10212A69	.47 mf 10% 100V mtlz poly
C34	8S10191A32	.047 mf 10% 160V polyester
C35	8S10191B98	.01 mf 10% 250V polyester
C36	23S10255A60	100 mf 63V Lytic
C37	8S10212A20	2.2 mf 10% 100V mtlz poly
C38	8S10212A20	2.2 mf 10% 100V mtlz poly
C39	8S10191B67	.22 mf 10% 250V polyester
C40	8S10212A10	1.0 mf 10% 100V mtlz poly (Use 8S10191A46)
C41	8S10064A06	.01 mf 10% 600V Mylar
C42	21S180A71	470 pf 10% 500V X5F
C43	23C65807A47	400 mf/125V; 600 mf/100V; 200 mf/50V; 20 mf/200V Lytic
C44	21S180E60	.01 mf +80–20% 50V Z5V
C45	21S10330A05	.0015 mf 20% 1.4KV Z5U
C47	23S10255A11	2000 mf 35V Lytic
C48	23S10255A30	1500 mf 30V Lytic
C49	23S10255A31	470 mf 40V Lytic
C51	*8S10191C49	.33 mf 10% 100V polyester
C52	8S10191C49	.33 mf 10% 100V polyester

DIODES & RECTIFIERS

REF. NO.	PART NUMBER	DESCRIPTION
D1	48S134921	DIODE, silicon: D1D; damper
D2	48S134978	DIODE, silicon: D1K; pulse limiter
D3	48D67120A11	DIODE, low power
D4	48S137114	RECTIFIER, H.V.: silicon; D2Y
D5	48S191A05	RECTIFIER, silicon: 91A05 (Use 48S191A07)
D6	48S137266	DIODE, silicon: zener; D4H
D7	48S134917	DIODE, dual: D1C; AFC
D8	48D67120A11	DIODE, low power
D9	48S191A05	RECTIFIER, silicon: 91A05 (Use 48S191A07)
D10	48S191A05	RECTIFIER, silicon: 91A05 (Use 48S191A07)
D11	48S191A05	RECTIFIER, silicon: 91A05 (Use 48S191A07)
D12	48S191A05	RECTIFIER, silicon: 91A05 (Use 48S191A07)
D13	48D67120A11	DIODE, low power
D15	48S191A05	RECTIFIER, silicon: 91A05 (Use 48S191A07)
D16	48S191A05	RECTIFIER, silicon: 91A05 (Use 48S191A07)
D17	48S191A05	RECTIFIER, silicon: 91A05 (Use 48S191A07)
D18	48S191A05	RECTIFIER, silicon: 91A05 (Use 48S191A07)

FUSES

REF. NO.	PART NUMBER	DESCRIPTION
F1	65S139183	FUSE: 1A-125V

INTEGRATED CIRCUITS

REF. NO.	PART NUMBER	DESCRIPTION
IC1	*51S10707A01	INTEGRATED CIRCUIT: T2Z

COILS & CHOKES

REF. NO.	PART NUMBER	DESCRIPTION
L1	24D68822A08	HORIZ SET
L2	24D68801A67	COMPENSATING: 2000 mh
L3	24D69163A18	HORIZ LINEARITY
L4	24V25000A74	HORIZ WIDTH: incls C42 & R68
L5	24D68523A15	DEFLECTION YOKE

TRANSISTORS

REF. NO.	PART NUMBER	DESCRIPTION
Q1	48S137171	1ST VIDEO: A6H
Q2	48S137127	2ND VIDEO: P2S
Q3	48S134919	VIDEO OUTPUT: A1M
Q4	48S137317	VIDEO DRIVER: A8H
Q5	48S137115	SYNC SEPARATOR: A5U
Q6	48S137172	HORIZ OSCILLATOR: A6J
Q7	48S137127	HORIZ PULSE SHAPER: P2S
Q8	48S137093	HORIZ DRIVER: A5F
Q9	48S134995	HORIZ OUTPUT: A6Z
Q10	48S137173	VERT OSCILLATOR (1): P2W
Q11	48S137171	VERT OSCILLATOR (2): A6H
Q12	48S137115	VERT DRIVER: A5U
Q13	48S134900	VERT OUTPUT: A1C
Q14	48S134952	REGULATOR DRIVER: A2J
Q15	48S137315	REFERENCE AMP: A8G
Q16	48S137368	REGULATOR: A8W
Q17	48S137172	AUDIO DRIVER: A6J
Q18	48S137168	AUDIO OUTPUT: P2V

CONTROLS

REF. NO.	PART NUMBER	DESCRIPTION
R5	18D68222A34	CONTRAST: 250 ohms
R10	18D66401A54	VIDEO BIAS: 4K
R17	18D67858A12	FOCUS: 2 meg
R21	*18D68222A35	BRIGHTNESS: 200K
R34	18D68222A37	HORIZ HOLD: 25K
R59	18D66401A54	VERT LINEARITY: 4K
R65	17D65820A38	VERT SIZE: 15 ohms
R74	17D65820A37	REGULATOR ADJUST: 2K
R82	18D68222A36	VERT HOLD: 3K
R85	18D68222A34	VOLUME: 250 ohms

RESISTORS

REF. NO.	PART NUMBER	DESCRIPTION
R2	6S125568	22K 10 ½W
R3	6S127541	56K 10% ½W
R4	6S127633	470 10% ½W
R6	6S128955	1500 10% 1W
R7	6S121847	4700 10% ½W
R8	6S122445	1800 10% ½W
R9	6S119926	2700 10% ½W
R11	6S128226	120 10% ½W
R12	6S127633	470 10% ½W
R13	*17S10731A01	3900 5% 5W WW
R14	6S127516	82 10% ½W
R15	6S131412	56 10% ½W
R18	– – – –	Part of CRT Socket Assembly
R19	– – – –	Part of CRT Socket Assembly
R20	– – – –	Part of CRT Socket Assembly
R22	6S129296	270K 10% ½W
R23	6S10053C67	27K 5% ½W
R24	6S127538	3.3 meg 10% ½W
R25	6S121300	27K 10% ½W
R26	6S127541	56K 10% ½W
R27	6S129875	2200 10% ½W
R28	6S125531	180K 10% ½W
R29	6S125531	180K 10% ½W
R30	6S125892	47K 10% ½W
R31	6S125534	100K 10% ½W
R32	6S124506	3300 10% ½W
R33	6S10053C53	6800 5% ½W
R35	6S127541	56K 10% ½W
R36	6S125545	390 10% ½W
R37	6S121301	1000 10% ½W
R38	6S10053C33	1000 5% ½W
R39	6S127516	82 10% ½W
R40	6S127547	1000 10% 1W
R41	6S127099	220 10% ½W
R42	6S127513	1500 10% ½W
R43	17S10130B07	1500 10% 3W fxd mtl film
R44	17S10159A04	4.7 10% 2W WW
R45	6S120141	150K 10% 1W
R46	6S127634	33K 10% 1W
R47	6S129417	1.5 meg 10% ½W
R48	6S10053D21	4.7 meg 10% ½W
R49	6S124797	150 10% ½W
R50	6S10053C45	3300 5% ½W
R52	6S124506	3300 10% ½W
R53	6S129874	68 10% ½W
R54	6S131972	39 10% ½W
R55	6S10053C65	22K 5% ½W
R57	6S119930	6800 10% ½W
R58	6S129793	82K 5% ½W
R60	6S122445	1800 10% ½W
R61	6S10053F29	820 10% 1W
R62	6S127005	5600 10% ½W
R63	6S121301	1000 10% ½W
R64	6S10053F17	10 10% 1W
R66	6S129064	4700 10% 1W

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REF. NO.	PART NUMBER	DESCRIPTION
R67	6S122848	18K 10% ½W
R68	6S124797	150 10% ½W
R69	17S647132	1200 10% 3W WW (Use 17S136197)
R71	6S119926	2700 10% ½W
R72	6S124551	15K 10% ½W
R73	6S129875	2200 10% ½W
R75	6S121301	1000 10% ½W
R76	6S124506	3300 10% ½W
R77	6S129221	100 10% ½W
R78	6S127005	5600 10% ½W
R79	17S135589	150 10% 10W WW
R81	6C66263A08	VARISTOR (Use 6S66263A16)
R86	6S124797	150 10% ½W
R87	17S135977	14 10% 5W WW
R88	6S121301	1000 10% ½W
R89	– – – –	Part of CRT Socket

TRANSFORMERS

REF. NO.	PART NUMBER	DESCRIPTION
T1	25D67440A03	HORIZ DRIVER
T2	*24D69791B17	H. V. TRANSFORMER: complete
T3	25D65840A22	VERT OUTPUT (Use 25D65840B23)
T4	25D68164A27	POWER

MISCELLANEOUS ELECTRICAL PARTS

REF. NO.	PART NUMBER	DESCRIPTION
V1	20WP4	CRT
	50D68384A02	SPEAKER: 4" PM

MECHANICAL PARTS

REF. NO.	PART NUMBER	DESCRIPTION
	*9D66133A34	CAP, SS Rectifier (H.V. Transf pri/sec lead)
	42B25158A01	CLAMP, metal: defl yoke mtg
	42D65864A54	CONNECTOR, 2nd anode
	31D70080B04	CONNECTOR, PC panel: 9 Contact; on chassis
P1	15S10183A22	CONNECTOR, plug: 10 Contact; less contacts (power)
	39S10184A52	CONTACT, plug: for power connector 15S10183A22
	5B69911A01	GROMMET, plastic: PC panel mtg
	26C66745A05	HEAT SINK: Q3
	14A562353	INSULATOR, mica; transistor socket: Q9, Q13, & Q16 (Use 14A543810)
	14C68842A04	INSULATOR, molded rubber: SS rect cap/H. V. transf
	*14S10550A02	INSULATOR, transistor cover: Q16
	2S7051	NUT, hex: 3/8-32; ctrl mtg
	5S10281A03	RIVET, drive pin: nylon; H. V. transf mtg
	47C66082A04	ROD, adjustment: width coil; L4
	3S136050	SCREW, tpg: 6-20 x ½ clu pan hd; Q9, Q13, Q16 & IC mtg
	*9D67555B27	SOCKET, CRT: incls leads & resistors
	9S10548A01	SOCKET, fuse: F1
	9C63825A01	SOCKET, IC & transistor: Q9, Q13, Q16 & IC1
	41D65987A01	SPRING, special: CRT aquadag grnd

MODEL XM500-11 - CHASSIS C19VP102

ELECTRICAL PARTS

REF. NO.	PART NUMBER	DESCRIPTION
	*1Y25016A89	MONITOR PANEL: "V28A"; complete KT346KM

CAPACITORS

REF. NO.	PART NUMBER	DESCRIPTION
C1	23C65282A41	50 mf 50V Lytic
C2	23C65282A41	50 mf 50V Lytic
C3	21S180D10	220 pf 20% 100V X5F (Use 21R132503)
C4	23C65282A41	50 mf 50V Lytic
C5	21S180E78	270 pf 10% 500V X5F
C6	23S10255A78	470 mf 16V Lytic
C7	21S180E78	270 pf 10% 500V X5F
C8	21S180B53	470 pf 10% 500V X5F
C10	8S10191B67	.22 mf 10% 250V polyester
C11	8S10191A54	.0068 mf 10% 160V polyester
C12	21S180D10	220 pf 20% 100V X5F (Use 21R132503)
C13	21R132503	220 pf 10% 100V X5F
C15	21S180C41	.0027 mf 10% 500V Z5F (Use 21K121699)
C16	23S10229A07	1.0 mf +40–20% 15V Lytic (Use 23C43280A17)
C17	8S10191B90	.033 mf 10% 160V polyester
C18	8S10299A73	.01 mf 10% 100V poly carb
C19	8S10299A74	.0082 mf 10% 160V poly carb
C20	8S10191B98	.01 mf 10% 250V polyester
C21	21S180B51	.001 mf 10% 500V X5F
C22	8S10191B98	.01 mf 10% 160V polyester
C23	21S180C52	18 pf 5% 500V NPO
C24	23D65282A40	150 mf 10V Lytic
C25	21S180B51	.001 mf 10% 500V X5F
C26	8S10212B53	.47 mf 10% 630V mtlz poly
C27	8S10212A11	1.0 mf 10% 630V mtlz poly
C28	8S10571A06	.01 mf 5% 1200V poly prop foil
C29	8S10212D33	.56 mf 10% 250V mtlz poly
C30	8S10191A32	.047 mf 10% 250V polyester
C31	21S180B87	220 pf 10% 500V X5F
C32	21S180D34	.005 mf 20% 1KV Z5F (Use 21S180D31)
C33	8S10212A69	.47 mf 10% 100V mtlz poly
C34	8S10191A32	.047 mf 10% 160V polyester
C35	8S10191B98	.01 mf 10% 250V polyester
C36	23S10255A60	100 mf 63V Lytic
C37	8S10212A20	2.2 mf 10% 100V mtlz poly
C38	8S10212A20	2.2 mf 10% 100V mtlz poly
C39	8S10191B67	.22 mf 10% 250V polyester
C40	8S10212A10	1.0 mf 10% 100V mtlz poly (Use 8S10191A46)
C41	8S10064A06	.01 mf 10% 600V Mylar
C42	21S180A71	470 pf 10% 500V X5F
C43	23C65807A47	400 mf/125V; 600 mf/100V; 200 mf/50V; 20 mf/200V Lytic
C44	21S180E60	.01 mf +80–20% 50V Z5V
C45	21S10330A05	.0015 mf 20% 1.4KV Z5U
C47	23S10255A11	2000 mf 35V Lytic
C48	23S10255A30	1500 mf 30V Lytic
C49	23S10255A31	470 mf 40V Lytic
C50	23D65282A41	50 mf 50V Lytic
C51	*8S10191C49	.33 mf 10% 100V polyester
C52	8S10191C49	.33 mf 10% 100V polyester

DIODES & RECTIFIERS

REF. NO.	PART NUMBER	DESCRIPTION
D1	48S134921	DIODE, silicon: D1D; damper
D2	48S134978	DIODE, silicon: D1K; pulse limiter
D3	48D67120A11	DIODE, low power
D4	48S137114	RECTIFIER, H.V.: silicon; D2Y
D5	48S191A05	RECTIFIER, silicon: 91A05 (Use 48S191A07)
D6	48S137266	DIODE, silicon: zener; D4H
D7	48S134917	DIODE, dual: D1C; AFC
D8	48D67120A11	DIODE, low power
D9	48S191A05	RECTIFIER, silicon: 91A05 (Use 48S191A07)
D10	48S191A05	RECTIFIER, silicon: 91A05 (Use 48S191A07)
D11	48S191A05	RECTIFIER, silicon: 91A05 (Use 48S191A07)
D12	48S191A05	RECTIFIER, silicon: 91A05 (Use 48S191A07)
D13	48D67120A11	DIODE, low power
D15	48S191A05	RECTIFIER, silicon: 91A05 (Use 48S191A07)
D16	48S191A05	RECTIFIER, silicon: 91A05 (Use 48S191A07)
D17	48S191A05	RECTIFIER, silicon: 91A05 (Use 48S191A07)
D18	48S191A05	RECTIFIER, silicon: 91A05 (Use 48S191A07)
D19	48D67120A11	DIODE, low power

FUSES

REF. NO.	PART NUMBER	DESCRIPTION
F1	65S138725	FUSE: .6A-125V
F2	65S138725	FUSE: .6A-125V

INTEGRATED CIRCUITS

REF. NO.	PART NUMBER	DESCRIPTION
IC1	*51S10707A01	INTEGRATED CIRCUIT: T2Z

COILS & CHOKES

REF. NO.	PART NUMBER	DESCRIPTION
L1	24D68822A08	HORIZ SET
L2	24D68801A67	COMPENSATING: 2000 uh
L3	24D69163A18	HORIZ LINEARITY
L4	24V25000A74	HORIZ WIDTH: incls C42 & R68
L5	24D68523A15	DEFLECTION YOKE

TRANSISTORS

REF. NO.	PART NUMBER	DESCRIPTION
Q1	48S137171	1ST VIDEO: A6H
Q2	48S137127	2ND VIDEO: P2S

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REF. NO.	PART NUMBER	DESCRIPTION
Q3	48S134919	VIDEO OUTPUT: A1M
Q4	48S137317	VIDEO DRIVER: A8H
Q5	48S137115	SYNC SEPARATOR: A5U
Q6	48S137172	HORIZ OSCILLATOR: A6J
Q7	48S137127	HORIZ PULSE SHAPER: P2S
Q8	48S137093	HORIZ DRIVER: A5F
Q9	48S134995	HORIZ OUTPUT: A6Z
Q10	48S137173	VERT OSCILLATOR (1): P2W
Q11	48S137171	VERT OSCILLATOR (2): A6H
Q12	48S137115	VERT DRIVER: A5U
Q13	48S134900	VERT OUTPUT: A1C
Q14	48S134952	REGULATOR DRIVER: A2J
Q15	48S137315	REFERENCE AMP: A8G
Q16	48S137368	REGULATOR: A6J
Q17	48S137172	AUDIO DRIVER: A6J
Q18	48S137168	AUDIO OUTPUT: P2V

CONTROLS

REF. NO.	PART NUMBER	DESCRIPTION
R5	18D68222A34	CONTRAST: 250 ohms
R10	18D66401A54	VIDEO BIAS: 4K
R17	18D67858A12	FOCUS: 2 meg
R21	*18D68222A35	BRIGHTNESS: 200K
R34	18D68222A37	HORIZ HOLD: 25K
R59	18D66401A54	VERT LINEARITY: 4K
R65	17D65820A38	VERT SIZE: 15 ohms
R74	17D65820A37	REGULATOR ADJUST: 2K
R82	18D68222A36	VERT HOLD: 3K
R85	18D68222A34	VOLUME: 250 ohms

RESISTORS

REF. NO.	PART NUMBER	DESCRIPTION
R1	6S127513	1500 10% ½W
R2	6S125568	22K 10 ½W
R3	6S127541	56K 10% ½W
R4	6S127633	470 10% ½W
R6	6S128955	1500 10% 1W
R7	6S121847	4700 10% ½W
R8	6S122445	1800 10% ½W
R9	6S119926	2700 10% ½W
R11	6S128226	120 10% ½W
R12	6S127633	470 10% ½W
R13	*17S10731A01	3900 5% 5W WW
R14	6S127516	82 10% ½W
R15	6S131412	56 10% ½W
R18	– – – –	Part of CRT Socket Assembly
R19	– – – –	Part of CRT Socket Assembly
R20	– – – –	Part of CRT Socket Assembly
R22	6S129296	270K 10% ½W
R23	6S10053C67	27K 5% ½W
R24	6S127538	3.3 meg 10% ½W
R25	6S121300	27K 10% ½W
R26	6S127541	56K 10% ½W
R27	6S121301	1000 10% ½W
R28	6S125531	180K 10% ½W
R29	6S125531	180K 10% ½W
R30	6S125892	47K 10% ½W
R31	6S125534	100K 10% ½W
R32	6S124506	3300 10% ½W
R33	6S10053C53	6800 5% ½W
R35	6S127541	56K 10% ½W
R36	6S125545	390 10% ½W
R37	6S121301	1000 10% ½W
R38	6S10053C33	1000 5% ½W
R39	6S127516	82 10% ½W
R40	6S127547	1000 10% 1W
R41	6S127099	220 10% ½W
R42	6S127513	1500 10% ½W
R43	17S10130B07	1500 10% 3W fxd mtl film
R44	17S10159A04	4.7 10% 2W WW
R45	6S120141	150K 10% 1W
R46	6S127634	33K 10% 1W
R47	6S129417	1.5 meg 10% ½W
R48	6S10053D21	4.7 meg 10% ½W
R49	6S124797	150 10% ½W
R50	6S10053C45	3300 5% ½W
R52	6S124506	3300 10% ½W
R53	6S129874	68 10% ½W
R54	6S131972	39 10% ½W
R55	6S10053C65	22K 5% ½W
R57	6S119930	6800 10% ½W
R58	6S129793	82K 5% ½W
R60	6S122445	1800 10% ½W
R61	6S10053F29	820 10% 1W
R62	6S127005	5600 10% ½W
R63	6S121301	1000 10% ½W
R64	6S10053F17	10 10% 1W
R66	6S129064	4700 10% 1W
R67	6S122848	18K 10% ½W
R68	6S124797	150 10% ½W
R69	17S647132	1200 10% 3W WW (Use 17S136197)
R71	6S119926	2700 10% ½W
R72	6S124551	15K 10% ½W
R73	6S129875	2200 10% ½W
R75	6S121301	1000 10% ½W
R76	6S124506	3300 10% ½W
R77	6S129221	100 10% ½W
R78	6S127005	5600 10% ½W
R79	17S135589	150 10% 10W WW
R81	6C66263A08	VARISTOR (Use 6S66263A16)
R86	6S124797	150 10% ½W
R87	17S135977	14 10% 5W WW
R88	6S121301	1000 10% ½W
R89	– – – –	Part of CRT Socket

SWITCHES

REF. NO.	PART NUMBER	DESCRIPTION
SW1	40S10624A01	SWITCH, slide: DP DT (115V-230V)

TRANSFORMERS

REF. NO.	PART NUMBER	DESCRIPTION
T1	25D67440A03	HORIZ DRIVER
T2	*24D69791B17	H. V. TRANSFORMER: complete
T3	25D65840A22	VERT OUTPUT (Use 25D65840B23)
T4	25D68164A27	POWER

MISCELLANEOUS ELECTRICAL PARTS

REF. NO.	PART NUMBER	DESCRIPTION
V1	20WP4	CRT
	50D68384A02	SPEAKER: 4" PM

MECHANICAL PARTS

REF. NO.	PART NUMBER	DESCRIPTION
	*9D66133A34	CAP, SS Rectifier (H.V. Transf pri/sec lead)
	42B25158A01	CLAMP, metal: defl yoke mtg
	42D65864A54	CONNECTOR, 2nd anode
	31D70080B04	CONNECTOR, PC panel: 9 Contact; on chassis
P1	15S10183A22	CONNECTOR, plug: 10 Contact; less contacts (power)
	39S10184A52	CONTACT, plug: for power connector 15S10183A22
	15S10630A01	COVER, nylon: slide switch; SW1
	5B69911A01	GROMMET, plastic: PC panel mtg
	26C66745A05	HEAT SINK: Q3
	14A562353	INSULATOR, mica; transistor socket: Q9, Q13, & Q16 (Use 14A543810)
	14C68842A04	INSULATOR, molded rubber: SS rect cap/H. V. transf
	*14S10550A02	INSULATOR, transistor cover: Q16
	2S7051	NUT, hex: 3/8-32; ctrl mtg
	5S10281A03	RIVET, drive pin: nylon; H. V. transf mtg
	47C66082A04	ROD, adjustment: width coil; L4
	3S136050	SCREW, tpg: 6-20 x ½ clu pan hd; Q9, Q13, Q16 & IC mtg
	*9D7555B27	SOCKET, CRT: incls leads & resistors
	9S10548A02	SOCKET, fuse: dual; F1 & F2
	9C63825A01	SOCKET, IC & transistor: Q9, Q13, Q16 & IC1
	41D65987A01	SPRING, special: CRT aquadag grnd

MODEL XM700-10-CHASSIS 23VP102

ELECTRICAL PARTS

REF. NO.	PART NUMBER	DESCRIPTION
	1Y25016A96	MONITOR PANEL: "V30A"; complete KT361LM

CAPACITORS

REF. NO.	PART NUMBER	DESCRIPTION
C1	23C65282A41	50 mf 50V Lytic
C2	23C65282A41	50 mf 50V Lytic
C3	21S180D10	220 pf 20% 100V X5F (Use 21R132503)
C4	23C65282A41	50 mf 50V Lytic
C5	21S180E47	180 pf 10% 500V N150
C6	23S10255A78	470 mf 16V Lytic
C7	21S180C01	680 pf 10% 500V X5F
C8	21S180B85	560 pf 10% 500V X5F
C10	8S10191B67	.22 mf 10% 250V polyester
C11	8S10191A54	.0068 mf 10% 160V polyester
C12	21S180D10	220 pf 20% 100V X5F (Use 21R132503)
C13	21S180B51	.001 mf 10% 500V X5F
C15	21S180C41	.0027 mf 10% 500V Z5F (Use 21K121699)
C16	23S10229A07	1.0 mf +40–20% 15V Lytic (Use 23C43280A17)

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REF. NO.	PART NUMBER	DESCRIPTION
C17	8S10191B90	.033 mf 10% 160V polyester
C18	8S10299A73	.01 mf 10% 100V poly carb
C19	8S10299A74	.0082 mf 10% 160V poly carb
C20	8S10191B98	.01 mf 10% 250V polyester
C21	21S180B51	.001 mf 10% 500V X5F
C22	8S10191B98	.01 mf 10% 160V polyester
C24	23D65282A40	150 mf 10V Lytic
C25	21S180B51	.001 mf 10% 500V X5F
C26	8S10212B53	.47 mf 10% 630V mtlz poly
C27	8S10212A11	1.0 mf 10% 630V mtlz poly
C28	8S10571A06	.01 mf 5% 1200V poly prop foil
C29	8S10212D33	.56 mf 10% 250V mtlz poly
C30	8S10191A32	.047 mf 10% 250V polyester
C31	21S180B87	220 pf 10% 500V X5F
C32	21S180D34	.005 mf 20% 1KV Z5F (Use 21S180D31)
C33	8S10212A69	.47 mf 10% 100V mtlz poly
C34	8S10191A32	.047 mf 10% 160V polyester
C35	8S10191B98	.01 mf 10% 250V polyester
C36	23S10255A60	100 mf 63V Lytic
C37	8S10212A20	2.2 mf 10% 100V mtlz poly
C38	8S10212A20	2.2 mf 10% 100V mtlz poly
C39	8S10191B67	.22 mf 10% 250V polyester
C40	8S10212A10	1.0 mf 10% 100V mtlz poly (Use 8S10191A46)
C41	8S10064A06	.01 mf 10% 600V Mylar
C42	21S180A71	470 pf 10% 500V X5F
C43	23C65807A47	400 mf/125V; 600 mf/100V; 200 mf/50V; 20 mf/200V Lytic
C44	21S180E60	.01 mf +80–20% 50V Z5V
C45	21S10330A05	.0015 mf 20% 1.4KV Z5U
C47	23S10255A11	2000 mf 35V Lytic
C48	23S10255A30	1500 mf 30V Lytic
C49	23S10255A31	470 mf 40V Lytic
C50	23D65282A41	50 mf 50V Lytic
C51	8S10191C49	.33 mf 10% 100V polyester
C52	8S10191C49	.33 mf 10% 100V polyester

DIODES & RECTIFIERS

D1	48S134921	DIODE, silicon: D1D; damper
D2	48S134978	DIODE, silicon: D1K; pulse limiter
D3	48D67120A11	DIODE, low power
D4	48S137114	RECTIFIER, H.V.: silicon; D2Y
D5	48S191A05	RECTIFIER, silicon: 91A05 (Use 48S191A07)
D6	48S137266	DIODE, silicon: zener; D4H
D7	48S134917	DIODE, dual: D1C; AFC
D8	48D67120A11	DIODE, low power
D9	48S191A05	RECTIFIER, silicon: 91A05 (Use 48S191A07)
D10	48S191A05	RECTIFIER, silicon: 91A05 (Use 48S191A07)
D11	48S191A05	RECTIFIER, silicon: 91A05 (Use 48S191A07)
D12	48S191A05	RECTIFIER, silicon: 91A05 (Use 48S191A07)
D13	48D67120A11	DIODE, low power
D15	48S191A05	RECTIFIER, silicon: 91A05 (Use 48S191A07)
D16	48S191A05	RECTIFIER, silicon: 91A05 (Use 48S191A07)
D17	48S191A05	RECTIFIER, silicon: 91A05 (Use 48S191A07)
D18	48S191A05	RECTIFIER, silicon: 91A05 (Use 48S191A07)
D19	48D67120A11	DIODE, low power

FUSES

F1	65S138725	FUSE: .6A-125V
F2	65S138725	FUSE: .6A-125V

INTEGRATED CIRCUITS

IC1	51S10707A01	INTEGRATED CIRCUIT: T2Z

COILS & CHOKES

L1	24D68822A08	HORIZ SET
L2	24D68801A67	COMPENSATING: 2000 mh
L3	24D69163A18	HORIZ LINEARITY
L4	24V25000A74	HORIZ WIDTH: incls C42 & R68
L5	24D68523A15	DEFLECTION YOKE

TRANSISTORS

Q1	48S137171	1ST VIDEO: A6H
Q2	48S137127	2ND VIDEO: P2S
Q3	48S134919	VIDEO OUTPUT: A1M
Q4	48S137317	VIDEO DRIVER: A8H
Q5	48S137115	SYNC SEPARATOR: A5U
Q6	48S137172	HORIZ OSCILLATOR: A6J
Q7	48S137127	HORIZ PULSE SHAPER: P2S
Q8	48S137093	HORIZ DRIVER: A5F
Q9	48S134995	HORIZ OUTPUT: A6Z
Q10	48S137173	VERT OSCILLATOR (1): P2W
Q11	48S137171	VERT OSCILLATOR (2): A6H
Q12	48S137115	VERT DRIVER: A5U

REF. NO.	PART NUMBER	DESCRIPTION
Q13	48S134900	VERT OUTPUT: A1C
Q14	48S134952	REGULATOR DRIVER: A2J
Q15	48S137315	REFERENCE AMP: A8G
Q16	48S137368	REGULATOR: A8W
Q17	48S137172	AUDIO DRIVER: A6J
Q18	48S137168	AUDIO OUTPUT: P2V

CONTROLS

R5	18D68222A34	CONTRAST: 250 ohms
R10	18D66401A54	VIDEO BIAS: 4K
R17	18D67858A12	FOCUS: 2 meg
R21	18D68222A35	BRIGHTNESS: 200K
R34	18D68222A37	HORIZ HOLD: 25K
R59	18D66401A54	VERT LINEARITY: 4K
R65	17D65820A38	VERT SIZE: 15 ohms
R74	17D65820A37	REGULATOR ADJUST: 2K
R82	18D68222A36	VERT HOLD: 3K
R85	18D68222A34	VOLUME: 250 ohms

RESISTORS

R1	6S127633	470 10% ½W
R2	6S125568	22K 10 ½W
R3	6S127541	56K 10% ½W
R4	6S127633	470 10% ½W
R6	6S128955	1500 10% 1W
R7	6S121847	4700 10% ½W
R8	6S122445	1800 10% ½W
R9	6S119926	2700 10% ½W
R11	6S128226	120 10% ½W
R12	6S127633	470 10% ½W
R13	17S10731A02	7500 5% 5W WW
R14	6S124797	150 10% ½W
R15	6S131412	56 10% ½W
R18	– – – –	Part of CRT Socket Assembly
R19	– – – –	Part of CRT Socket Assembly
R20	– – – –	Part of CRT Socket Assembly
R22	6S129296	270K 10% ½W
R23	6S10053C67	27K 5% ½W
R24	6S127538	3.3 meg 10% ½W
R25	6S121300	27K 10% ½W
R26	6S127541	56K 10% ½W
R27	6S129875	2200 10% ½W
R28	6S125531	180K 10% ½W
R29	6S125531	180K 10% ½W
R30	6S125892	47K 10% ½W
R31	6S125534	100K 10% ½W
R32	6S124506	3300 10% ½W
R33	6S10053C53	6800 5% ½W
R35	6S127541	56K 10% ½W
R36	6S125545	390 10% ½W
R37	6S121301	1000 10% ½W
R38	6S10053C33	1000 5% ½W
R39	6S127516	82 10% ½W
R40	6S127547	1000 10% 1W
R41	6S127099	220 10% ½W
R42	6S127513	1500 10% ½W
R43	17S10130B07	1500 10% 3W fxd mtl film
R44	17S10159A04	4.7 10% 2W WW
R45	6S120141	150K 10% 1W
R46	6S127634	33K 10% 1W
R47	6S128229	680K 10% ½W
R48	6S10053D21	4.7 meg 10% ½W
R49	6S124797	150 10% ½W
R50	6S10053C45	3300 5% ½W
R52	6S124506	3300 10% ½W
R53	6S129874	68 10% ½W
R54	6S131972	39 10% ½W
R55	6S10053C65	22K 5% ½W
R57	6S119930	6800 10% ½W
R58	6S129793	82K 5% ½W
R60	6S129875	2200 10% ½W
R61	6S10053F29	820 10% 1W
R62	6S119930	6800 10% ½W
R63	6S121301	1000 10% ½W
R64	6S10053F17	10 10% 1W
R66	6S129064	4700 10% 1W
R67	6S122848	18K 10% ½W
R68	6S124797	150 10% ½W
R69	17S647132	1200 10% 3W WW (Use 17S136197)
R71	6S119926	2700 10% ½W
R72	6S124551	15K 10% ½W
R73	6S129875	2200 10% ½W
R75	6S121301	1000 10% ½W
R76	6S124506	3300 10% ½W
R77	6S129221	100 10% ½W
R78	6S127005	5600 10% ½W
R79	17S135589	150 10% 10W WW
R81	6C66263A08	VARISTOR (Use 6C66263A16)
R86	6S124797	150 10% ½W
R87	17S135977	14 10% 5W WW
R88	6S121301	1000 10% ½W
R89	– – – –	Part of CRT Socket

SWITCHES

SW1	40S10624A01	SWITCH, slide: DP DT (115V-230V)

MODEL XM700-10 - CHASSIS 23VP102 CONT'D ON NEXT PAGE

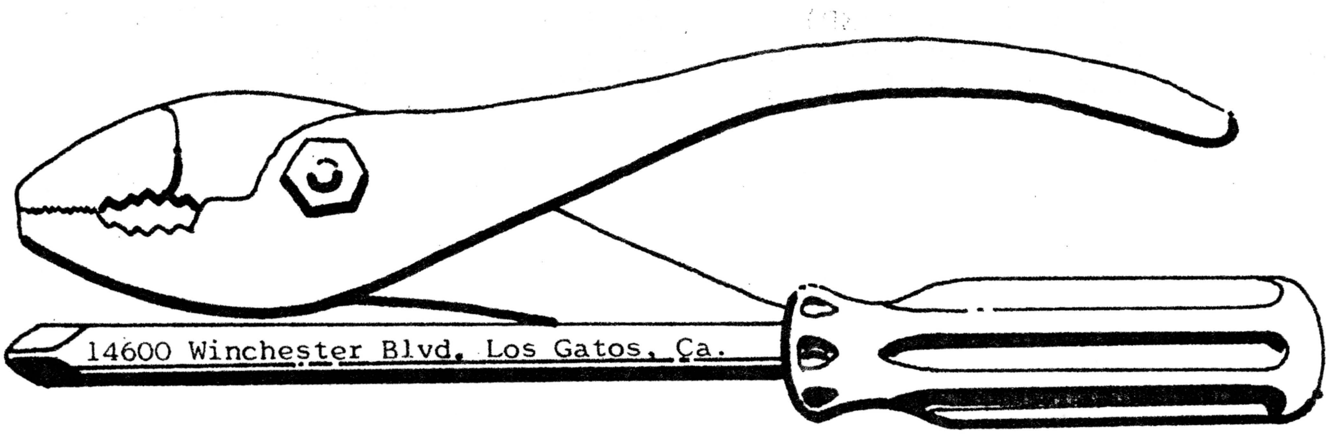
REF. NO.	PART NUMBER	DESCRIPTION
TRANSFORMERS		
T1	25D67440A03	HORIZ DRIVER
T2	*24D69791B17	H. V. TRANSFORMER: complete
T3	25D65840A22	VERT OUTPUT (Use 25D65840B23)
T4	25D68164A27	POWER
MISCELLANEOUS ELECTRICAL PARTS		
V1	23JEP4	CRT
	50D68384A02	SPEAKER: 4" PM
MECHANICAL PARTS		
	*9D66133A34	CAP, SS Rectifier (H.V. Transf pri/sec lead)
	42B25158A01	CLAMP, metal: defl yoke mtg
	42V25009A31	CONNECTOR, 2nd anode complete
	31D70080B04	CONNECTOR, PC panel: 9 Contact; on chassis
P1	15S10183A22	CONNECTOR, plug: 10 Contact; less contacts (power)
	39S10184A52	CONTACT, plug: for power connector 15S10183A22
	15S10630A01	COVER, nylon: slide switch; SW1
	5B69911A01	GROMMET, plastic: PC panel mtg
	26C66745A05	HEAT SINK: Q3
	14A562353	INSULATOR, mica; transistor socket: Q9, Q13, & Q16 (Use 14A543810)
	14C68842A04	INSULATOR, molded rubber: SS rect cap/H. V. transf
	14S10550A02	INSULATOR, transistor cover: Q16
	2S7051	NUT, hex: 3/8-32; ctrl mtg
	5S10281A03	RIVET, drive pin: nylon; H. V. transf mtg
	47C66082A04	ROD, adjustment: width coil; L4
	3S136050	SCREW, tpg: 6-20 x ½ clu pan hd; Q9, Q13, Q16 & IC mtg
	9D67555B27	SOCKET, CRT: incls leads & resistors
	9S10548A02	SOCKET, fuse: dual; F1 & F2
	9C63825A01	SOCKET, IC & transistor: Q9, Q13, Q16 & IC1
	41D65987A01	SPRING, special: CRT aquadag grnd

*DENOTES PARTS APPEARING IN ANY LIST FOR FIRST TIME

CUSTOMER SERVICE BULLETIN

Due to the increasing number of machines which are entering the field, our Customer Service personnel are becomming increasingly concerned that all service personnel will be able to obtain replacement parts. We have created a general information catalog which covers all past games and includes a complete parts list per game. All distributors should have a copy of this by now. If you don't have one, please call Bill Arkush at Atari.

Additionally, we have created a transistor cross reference guide for your convenience in locating active devices locally.



TELEDYNE PACKARD BELL COLOR TELEVISION

CHASSIS 98C38, 98C42, 98C44

Deflection Module DFM1

Q302	Horiz. Osc.	99S034	M331
Q303	Horiz. Predriver	99S077-1	MPS6517
Q304	Horiz. Driver	99S102-1	MPSU04
Q305	Sync. Splitter	99S070-1	MPSA06
Q306	Vert. Switch	99S060-1	2N4401
Q307	Vert. Predriver	99S061-1	2N5961
Q308	Vert. Driver	99S101-1	2N4924
Q309	Power	99S099-1	2N6107
Q310	Power	99S100-1	2N5496
Q311	Horiz. Output	99S079-1	Refer to Teledyne
Q312	Sync.	99S034	M321
			MSD6102

Power Supply Module RPM1

Q602	Transistor	99S103-1	RCA410 or DELCO 7934987
Q604	Transistor	99S083-1	2N5494

Audio Module AUM1

IC501	Removed from circuit		
Q502	Audio Driver	99S090-1	MPSA05
Q503	Audio Output	99S091-1	MPSU01
Q504	Audio Output	99S092-1	MPSU51

Video Module VIM1

Q701	2nd Video	99S036	M331
Q702	3rd Video	99S070-1	MPSA06
Q703	4th Video	99S033	MPC033
Q704	5th Video	99S084-1	2N2927
Q705	Vertical Blanker	99S034	M321
Q706	Video Output (RED)	99S063-1	MPSU10 or RCA2N6176
Q707	Video Output (Green)	99S063-1	MPSU10
Q708	Video Output (Blue)	99S063-1	MPSU10

HEAD OFFICE

Teledyne Packard Bell
12333 W. Olympic Blvd.
Los Angeles, Calif. 90064

TELEDYNE SERVICE COMPANY SERVICE CENTERS

Alhambra	2221 W. Valley Blvd.	CA.	91803	(213) 282-3195
Anaheim	626 N. Brookhurst	CA.	92801	(714) 772-6930
Atlanta	3381-A Lawrenceville Hwy	GA.	30084	(404) 939-2581
Baltimore	6826 Eastern Ave.	MD.	21224	(301) 633-3223
Belmont	1148 El Camino Real	CA.	94002	(415) 593-1615
Birmingham	2831 S. 18th St.	AL.	35209	(205) 871-9648
Burbank	2406 W. Olive Ave.	CA.	91506	(213) 845-7231
Camarillo	1760 Ventura Blvd.	CA.	93010	(805) 482-0739
Chicago	4435 N. Harlem Ave.	IL.	60656	(312) 457-1404
So. Chicago	1050 E. 162nd St., So. Holland	IL.	60473	(312) 333-6170
Costa Mesa	117 Cabrillo St.	CA.	92627	(714) 642-1650
Dallas	8383 Stemmons Freeway	TX.	75247	(214) 631-1534
Denver	454 S. Federal Blvd.	CO.	80219	(303) 935-2455
Drexel Hill	5060 State Rd.	PA.	19026	(215) 626-8300
Ft. Lauderdale	2000 N. Federal Hwy.	FL.	33305	(305) 566-5491
Ft. Worth	801 W. Magnolia	TX.	76104	(817) 921-3019
Granada Hills	17021 Chatsworth St.	CA.	91344	(213) 363-9535
Hollywood	600 N. La Brea Ave.	CA.	90036	(213) 936-7137
Honolulu	970 Ahua St.	HI.	96819	(808) 839-4588
Houston	6400 S.W. Freeway	TX.	77036	(713) 781-3656
Indianapolis	2837 Lafayette Rd.	IN.	46222	(317) 926-5337
Kansas City	7805 Troost	MO.	64131	(816) 523-0230
Long Beach	3110 E. Willow	CA.	90806	(213) 426-2581
Los Angeles	6833 E. Acco St.	CA.	90040	(213) 724-1150
Louisville	5057 Poplar Level Rd.	KY.	40219	(502) 964-3366
N. Miami	12601 N.E. 7th Ave.	FL.	33161	(305) 891-4701
S. Miami	9531 S.W. 160th St.	FL.	33157	(305) 233-7420
Milwaukee	2620 W. Whitaker Ave.	WI.	53221	(414) 282-2580
Minneapolis	670 W. 92nd St.	MN.	55420	(612) 881-8615
Moorestown	204 W. Route 38	NJ.	08057	(609) 234-1705
New York	32-75 Steinway St., L. I. City	NY.	11103	(212) 932-6010
Norfolk	6622 E. Virginia Beach Blvd.	VA.	23502	(804) 497-1021
Oakland	3655 Foothill Blvd.	CA.	94601	(415) 535-1100
Philadelphia	13631-33 Philmont Ave.	PA.	19116	(215) 677-6664
Phoenix	2816-A N. 16th St.	AZ.	85006	(602) 264-5241
Portland	1605 N.W. Everett	OR.	97209	(503) 222-9716
Riverside	3640 Rubidoux Blvd.	CA.	92509	(714) 686-6481
Rochester	3259 Winton Rd. So.	NY.	14623	(716) 275-9330
Sacramento	2314 "K" St.	CA.	95814	(916) 444-5691
San Antonio	1213 Basse Rd.	TX.	78212	(512) 736-4603
San Diego	7843 Clairmont Mesa Blvd.	CA.	92111	(714) 279-7161
San Francisco	625 Potrero	CA.	94110	(415) 285-5575
San Leandro	853 Fremont	CA.	94577	(415) 352-3910
Santa Clara	2415 De La Cruz Blvd.	CA.	95050	(408) 247-1636
Santa Monica	1609 Montana Ave.	CA.	90403	(213) 451-9892
St. Louis	10208 Manchester Rd.	MO.	63122	(314) 965-2200
Seattle	4415 Aurora Ave.	WA.	98103	(206) 633-0789
S. Seattle	15030 Military Rd. So.	WA.	98188	(206) 244-6900
South Gate	4478 Tweedy Blvd.	CA.	90280	(213) 566-2184
Syracuse	1966 Teall Ave.	NY.	13206	(315) 437-6582
Tacoma	2515 S. Tacoma Ave.	WA.	98402	(206) 272-2175
Tampa	4050 E. Hillsborough	FL.	33610	(813) 621-2431
Tarzana	6022 Reseda Blvd.	CA.	91356	(213) 345-9587
Torrance	1334 Post Ave.	CA.	90501	(213) 320-2575
Tucson	4226 Speedway Blvd.	AZ.	85712	(602) 327-3455
Walnut Creek	2033 N. Broadway	CA.	94596	(415) 937-0260
Westchester	8711 La Tijera	CA.	90045	(213) 670-4024
West Covina	2692 E. Garvey Ave.	CA.	91790	(213) 332-1126
Whittier	11212 E. Whittier Blvd.	CA.	90606	(213) 692-0671
Wichita	830 E. Murdock	KS.	67214	(316) 265-0781
Wichita Falls	3118 Seymour Hwy.	TX.	76301	(817) 723-7175
Yakima	803 Summitview	WA.	98902	(509) 453-0042

MOTOROLA MODEL XM 500-11 & XM 700-10

Circuit Designation	Device	MDP Part Number	Application	Motorola SPD Replacement Part	(2N) Equivalent
Q-1	T	482137171	1st Video: A6H		2N4400
Q-2	T	48S137127	2nd Video: P2S		2N4403
Q-3	T	48S134919	Video Output: A1M		2N3500
Q-4	T	48S137317	Video Driver: A8H		2N4400
Q-5	T	48S137172	Sync Separator: A6J		2N4400
Q-6	T	48S137317	Horiz. Oscillator: A5U		2N4400
Q-7	T	48S137127	Horix. Pulse Shaper: P2S		2N4403
Q-8	T	48S137093	Horiz. Driver: A5F		2N3500
Q-9	T	48S137203	Horiz. Output: A6Z	MJ3030 2N5157	2N3902
Q-10	T	48S137173	Vert. Oscillator (1): P2W		2N4403
Q-11	T	48S137171	Vert. Oscillator (2): A6H		2N4400
Q-12	T	48S137115	Vert. Driver: A5U		2N4400
Q-13	T	48S134900	Vert. Output: A1C	MJ3029	2N5151
Q-14	T	48S134952	Regulator Driver: A2J		2N4400
Q-15	T	48S137315	Reference Amp: A8G		2N4409
Q-16	T	48S137368	Regulator: A8W		2N3442
Q-17	T	48S137172	Audio Driver: A6J		2N4400
Q-18	T	48S134988	Audio Output: P2V		2N4030
ICI	IC	51S10707A01	5 V. Regulator: T2Z		
D-1	D	48S134921	Silicon: D1D; Damper		1N4007*
D-2	D	48S134978	Silicon: D1K; Pulse Limiter		1N4007*
D-3	D	48D67120A11	Low Power		1N4005
D-4	D	48S137114	H.V.; Sel D3S		VARO
D-5	R	48S191A05	Silicon; 91A05		1N4005
D-6 & 8	D	48D67130A11	Low Power		
D-7	D	48S134917	Dual; D1C; Detector	MSD6102	1N914**
D-9, 10, 11 & 12	D	48S191A05	Low Voltage Supply		2N4400

Motorola Display Products
Export and Parts
455 E. North Avenue
Carol Stream, Ill. 60187

Attention: Parts Dept.

(312) 690-1400

*Motorola Only
**2Required

ZENITH CHASSIS 19EB12

Device No.	Zenith P/N	Cross Reference	Manufacturer
Q201	121-713	NJ225	
A202	121-821	DTS0713 or 2SC1004	
	or	or ZSC642A	
	121-758	A702	
Q203	121-985	2SC643A	Toshiba
Q401	121-699	2N4248	
Q402	121-671	2N3569	
Q403	121-446	MPS6516	
Q404	121-895	SPS907 or EL438	Motorola
Q405	121-975	121-888 or EL403	Zenith/Motorola
	or		
Q703	121-982	121-888	Zenith
Q406	121-868	D40N3	GE
Q704	121-888	SPS2104 or X32C5198	Motorola/GE/F
		or TEH0147	
CR207	103-248	Information not available	
CR401-CR402	103-142-01	at this time.	
CR701-CR705		Will be supplied	
CR101	103-23	as soon as	
CR201	103-193	possible.	
CR202	103-239-02		
CR203-CR206	212-76		

For further information or to purchase parts directly from the factory, contact:

Zenith Radio Corp.
Export and Parts
1900 North Austin Avenue
Chicago, Illinois 60639

Attention: Mrs. Vigil

(312) 745-4993

ZENITH DISTRIBUTORS

Quick Reference Telephone Index

Telephone Number		
518-465-2351	Albany	Henzel-Powers, Inc.
505-243-7863	Albuquerque(El Paso Branch)	Albert Mathias & Co.,Inc.
806-376-4722	Amirillo	Amarillo Hardware Co.
404-691-0730	Atlanta	Graybar Electric, Inc.
301-644-2900	Baltimore	The Jos. M. Zamoiski Co.
319-359-1301	Bettendorf(Des Moines Branch)	A.A. Schneiderhahn Co.
406-248-7771	Billings	Midland Implement Co.,Inc.
205-252-3182	Birmingham	Hart-Greet, Inc.
716-633-8305	Buffalo (Cheektowaga). . .	Joseph Strauss Co., Inc.
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617-547-8000	Cambridge	Northeastern Distributors,Inc.
717-761-0241	Camp Hill	Peirce-Phelps, Inc.
304-342-1171	Charleston, W.Va.	Eskew, Smith & Cannon
704-344-8621	Charlotts	Allison-Erwin Company
615-266-4805	Chattanooga	McWhorter-Weaver & Co.
312-379-9400	Chicago (Northlake)	Zenith Radio Dist. Corp.
716-633-8305	Cheektowaga(Buffalo). . . .	Joseph Strauss Co.
513-853-6000	Cincinnati	The Knodel-Tygrett Co.
216-243-9900	Cleveland	Graybar Electric Co.,Inc.
803-256-7426	Columbia, S.C.(Charlotte)	Allison-Erwin Company
614-261-0331	Columbus	The Tracy-Wells Company
213-724-2400	Commerce (Los Angeles) . .	Sues, Young & Brown, Inc.
201-272-2800	Cranford	Zenith Radio Corp. of N.J.
214-691-5555	Dallas	The Stewart Company
513-224-9623	Dayton	V.J. McGranahan, Inc.
303-355-2345	Denver	McCollum-Law Corp.
515-244-3157	Des Moines	A.A. Schneiderhahn Co.
313-869-7900	Detroit	Radio Dist. Co.
915-533-1686	El Paso	Albert Mathias & Co.,Inc.
701-293-1811	Fargo(Minneapolis Branch)	Reinhard Brothers, Co.
501-782-8944	Ft. Smith	Taylor Distributing Co.,Inc.
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209-268-8544	Fresno	B.J. DeJarnatt Wholesale Co.
616-241-6581	Grand Rapids	J.A. White Dist. Co.
414-499-3171	Green Bay	Moreley-Murphy Co.
203-527-7107	Hartford(North Haven Br.).	The Plymouth Elec. Co.
314-731-4680	Hazelwood(St.Louis). . . .	Hollander & Co., Inc.
808-524-5533	Honolulu	VHY Home & Industrial Prod.
713-675-6521	Houston	Automatic Dist. Corp.
317-898-0670	Indianapolis	Rodefeld Co., Inc.
601-362-5464	Jackson	McKee & McRae, Inc.
904-356-4812	Jacksonville	Cain & Bultman, Inc.
814-266-8713	Johnstown	Cambria Equipment Co.
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304-453-3555	Kenova (Williamson Br.). .	Persinger Supply Co., Inc.
301-322-2000	Landover	The Jos. M. Zamoiski Co.
913-888-4800	Lenexa (Kansas City) . . .	Zenith Dist.Corp.of Kansas
501-376-2457	Little Rock	Graybar Elec. Co.

213-724-2400	Los Angeles(Commerce) . . .	Sues, Young & Brown, Inc.
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415-621-8545	San Francisco	Zenith Dist. Corp. of N.CA.
206-682-8282	Seattle	Seattle Pacific Sales Co.
318-423-0533	Shreveport	Tri-States Dist. Co.,Inc.
509-534-0611	Spokane	Columbia Electric
417-862-4475	Springfield	Hollander Dist. Co., Inc.
219-388-1458	South Bend(Ft.Wayne Br.). .	Wayne Hardware Co., Inc.
315-474-1251	Syracuse	Onondaga Supply Co., Inc.
813-229-6571	Tampa	Cain & Bultman, Inc.
812-232-0461	Terre Haute	Walker Electric Co., Inc.
419-241-8271	Toledo	McGranahan Distributing Co.
	Youngstown (Cleveland Br.).	Graybar Elec. Co., Inc.
301-322-2000	Washington (Landover) . . .	The Jos.M. Zamoiski Co.
316-263-2271	Wichita	The S.A. Long Company, Inc.
304-235-1400	Williamson	Persinger Supply Co.,Inc.

CANADIAN DISTRIBUTORS

902-667-3307	Amherst, Nova Scotia, Canada . .	Waldale Ltd.
403-253-7171	Calgary, Alberta	Bow River Equip.Ltd.
403-455-7171	Edmonton, Alberta	Bruce Robinson Elec.
514-342-0210	Montreal, Quebec	Zenith Radio Corp.of Can.
416-255-2324	Toronto, Canada	Zenith Radio Corp.of Can.
604-879-4631	Vancouver, B.C.	Major Appliances Div. of Acklands, Ltd.
204-783-7011	Winnipeg, Manitoba	Major Appliances Div. of Acklands, Ltd.

HITACHI SALES CORPORATION OF AMERICA
National Headquarters Office: 48-50 34th St.
Long Island City, N.Y. 11101
Tel. 212-361-3090

Eastern Regional Office: 4850 34th St. Long Island City, N.Y. 11101
Long Island City, N.Y. 11101
Tel. 212-361-3090

Mid-Western Regional Office: 1400 Morse Ave.
Elk Grove Villiage
Chicago, Ill. 60007
Tel. 312-593-7500

South-Western Regional Office: 1121 Round Table Dr.
Dallas, Texas 75247
Tel. 214-638-5820

Western Regional Office: 2550 Santa Fe Ave.
Redondo Beach, Calif. 90278
Tel. 213-644-3655

HITACHI SALES CORPORATION OF HAWAII
743-G Waiakamilo Rd.
Honolulu, Hawaii 96817
Tel. 808-841-0431

HITACHI SALES CORPORATION OF PANAMA
Edificio Vallarino
Calle 32
Avenida Justo Arosemena
Panama City, Panama
Tel. 25-0315,3899

MGA

MITSUBISHI INTERNATIONAL CORPORATION
7045 North Ridgeway Avenue
Linclonwood, Illinois 60645

ZENITH RADIO CORPORATION
1900 N. Austin Ave.
Chicago, Illinois

TRANSISTORS (for Hitachi)

C 3	TR 201	0573474	silicon	2SC682 A
C 4	TR 202	0573474	silicon	2SC682 A
C 4	TR 203	2320141	silicon	2SC717
C 5	TR 251	2320041	silicon	2SC460 B
C 6	TR 252	2320051	silicon	2SC856
B 4	TR 401	2320041	silicon	2SC460 B
B 5	TR 402	0573131	germanium	2SB77 C
B 5	TR 403	2320596	silicon	2SC458 C / D
A 6	TR 404	2320647	silicon	2SC1213 C D
B 6	TR 405	2320631	silicon	2SA673 B / C
D 5	TR 502	2320514	germanium	2SA15 V
E 3	TR 503	2320591	silicon	2SC458 B / C
D 4	TR 551	2320471	silicon	2SC535 B / C
D 4	TR 552	2320596	silicon	2SC458 C / D
E 4	TR 601	2320591	silicon	2SC458 B / C
E 4	TR 602	2320423	germanium	2SB77 C / D
E 5	TR 603	2320596	silicon	2SC458 C / D
D 5	TR 604	2320651	silicon	2SC1061 C
E 5	TR 605	0573166	germanium	2SB337 B
E 5	TR 701	0573480	silicon	2SC458 B
E 5	TR 702	2320631	silicon	2SA673 B / C
F 5	TR 703	0573212	germanium	2SB468
F 2	TR 901	2320541	germanium	2SB337 A / B
F 3	TR 902	2320646	silicon	2SC1213 B / C
C 5	CR 201	0275005	Diode-Germanium	1N60
D 5	CR 251	0575001	Diode-Germanium	1N34A
C 6	CR 252	2330351	Diode-Silicon	1S2076
A 4	CR 401	0575005	Diode-Germanium	1N60
B 4	CR 402	0575005	Diode-Germanium	1N60
D 5	CR 501	2330351	Diode-Silicon	1S2076
D 4	CR 551	0575001	Diode-Germanium	1N34A
D 4	CR 552	0575001	Diode-Germanium	1N34A
D 3	CR 553	0575001	Diode-Germanium	1N34A
E 4	CR 701	0575001	Diode-Germanium	1N34A
F 4	CR 702	0575001	Diode-Germanium	1N34A
F 6	CR 703	2330551	Diode-Silicon	V09C
D 6	CR 704	2330251	Diode-Silicon	V06C
F 6	CR 705	2330251	Diode-Silicon	V06C
F 6	CR 706	2330033	Diode-Silicon	HS20/1
F 2	CR 901	2330251	Diode-Silicon	V06C
F 2	CR 902	2330251	Diode-Silicon	V06C
F 2	CR 903	2330251	Diode-Silicon	V06C
F 2	CR 904	2330251	Diode-Silicon	V06C
F 3	CR 905	2330302	Diode-Zener	AW01-07

TRANSISTORS (CONT'D)

PLACE	SYMBOL NO.	STOCK NO.	DESCRIPTION	
D 4	TH 551	0576057	Thermistor	D-1E
D 3	TH 552	0576038	Thermistor	D-2B
E 5	TH 601	0576057	Thermistor	D-1E
A 5	VA 401	2330611	Varistor	HV46

TRANSISTORS & ICs - MGA

Q 101	260P24901	Silicon	NPN	2SC11871
Q 102	260P1760	"	"	2SC763
Q 103	260P13001	"	PNP	2SA353-AC
Q 201	260P06904	"	NPN	2SC454-B
Q 241	260P10301	"	"	2SC154C
"	260P22101	"	"	2SC1103
Q 401	260P21002	"	PNP	2SA15-V/R
Q 402	260P19503	"	NPN	2SC945
Q 403	260P19503	"	NPN	2SC945
Q 404	260P24803	"	"	2SC1161
Q 501	260P12002	"	"	2SC281-B
Q 502	260P12401	"	"	2SD204
Q 503	260P08901	"	"	2SC940
Q 701	260P14103	"	"	2SC458-C
Q 702	"	"	"	"
Q 703	260P07704	"	"	2SC712-D
Q 704	260P14102	"	"	2SC458-B
Q 705	260P07703	"	"	2SC712-CD
Q 706	"	"	"	"
Q 901	260P20101	"	"	2SD155
Q 902	260P04001	"	"	2SC620-C
IC 311	266P00103	Integrated Circuit		M5113P
IC 341	266P30201	Integrated Circuit		NPC200C

DIODES & OTHERS

D 101	264P01305	Germanium	1N60
D 102	264P00801	"	1N34A
D 103	264P01305	"	1N60
D 104	"	"	"
D 241	264P00801	"	1N34A
D 341	264P04705	Silicon	SR1FM-2 (BB-126)
D 401	"	"	"
D 501	264P01305	Germanium	IN60
D 502	"	"	"
D 503	"	"	"
D 504	264P09101	Silicon	FG2N
D 505	264P06603	"	SR1HM-8
D 506	264P08902	Selenium	US25/1AS
D 701	264P01305	Germanium	1N60
D 702	264P00801	"	1N34A
D 703	"	"	"
D 901	264P09001	Silicon	F14A
D 902	"	"	"
D 903	"	"	"
D 904	"	"	"
D 905	264P04003	"	RD16A (BB-126)

DIODES & OTHERS CONT'D

RV 401	265P01501	Varistor	SC-02
RV 402	265P03503	"	TVS-1/2D
RV 901	"	"	"
RT 401	265P00601	Thermistor	23D28

HAND TOOLS TYPE "A"

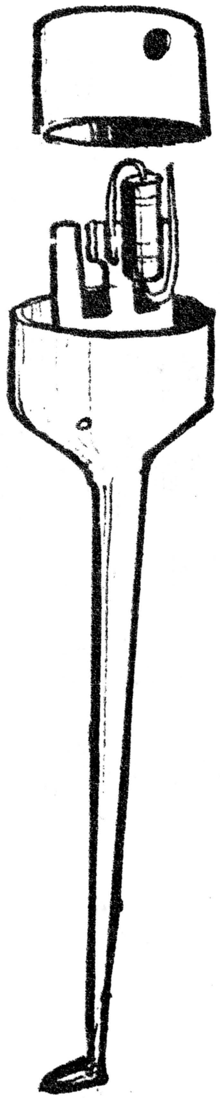
Manufacturer's Part No.	Manufacturers Name	Description	Manufacturer's Price
1. 4213	Union	Steel Utility Box, 13½"x 6½" x 5 5/8"	$3.38
2. 95AE	Erem	Diagonal Cutters	6.22
3. 11D	Erem	Long Narrow Chain nose	4.95
4. A90MS	Hunter	Tip-Dykes	6.64
5. "A"	Erem	Tweezers	3.71
6. MS-2	Hunter	Scribe	1.10
7. No. 1	Xacto	Knife	.65
8. No. 16	Xacto	Blades	.60
9. X-A30-6	Hunter	Pliers	1.81
10. 99-PS-40	Xcelite	Hex Kit	7.80
11. PS-140	Xcelite	Screw Driver Nut Compact Set	6.00
12. 99-PS-51MM	Xcelite	Nut Driver	9.45
13. W-TCP	Weller	Soldering Iron	26.15
14. WRAP	Kester	.031 Flux-Core Solder	4.18
15. SS011	Soldapullt	Solder Sucker	5.95
16. 40-4-5	Soder-Wick	#4 size	1.47
17. #880		IC Insertion Tool	4.95
18. No. 7	Master	Pad Lock	1.95
19. 47100	Amp	Super Champ (Wire Strippers)	7.05

RECOMMENDED TEST EQUIPMENT

Manufacturer's Part Number		Manufacturer's Name	Description	Manufacturer's Price
1.		Atari	Video Probe*	Consult Factory
2.		Atari	Universal Test Unit	Consult Factory
3.		Atari	Universal Test Unit Cables	Consult Factory
4.	D83	Telequipment	50MHZ Dual-Trace Oscillator	$ 800.00
5.	V4	Telequipment	Dual-Trace Amp for D83	295.00
6.	S2A	Telequipment	Dual Time Base for D83	400.00
7.	DM64	Telequipment	10MHZ Dual-Trace Oscillator	1,095.00
8.	465	Tektronix	100MHZ Dual-Trace Oscillator	1,725.00
9.	Option 5	Tektronix	TV Sync Separator	100.00
10.		Kurz-Kasch	LP-520 Logic Probe	69.95
11.		Kurz-Kasch	HL-582 Logic Pulser	89.95
12.		Atari	LP-600 TV Probe	69.95

* The Video Probe helps cut down the time it takes to test a board. It is made up of two easy hooks, 20 inches of 20 AWG wire and one 4.7K resistor in series with the wire. To use it, one end is connected to the negative side of the video coupling cap. Using the 4.7K resistor as a coupling resistor, put the other end on the signal you want to check. The signal will be coupled through the video signal and this can be seen on the screen of the TV. The signal will look like white or black lines on the screen. If that signal is not the correct one, the lines will be different or not visible. Compare this with a good board.

ATARI VIDEO PROBE

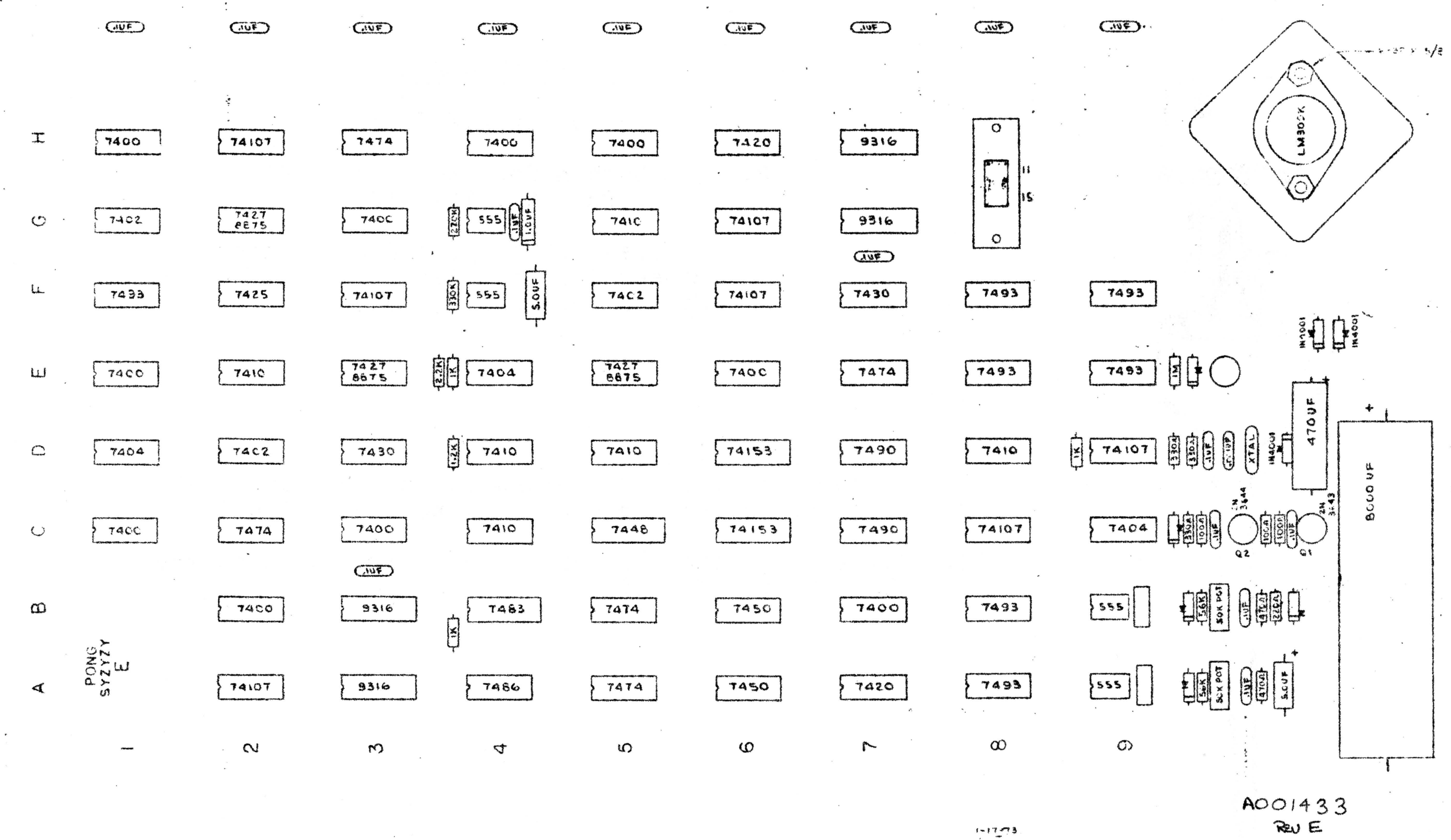


MATERIAL NEEDED

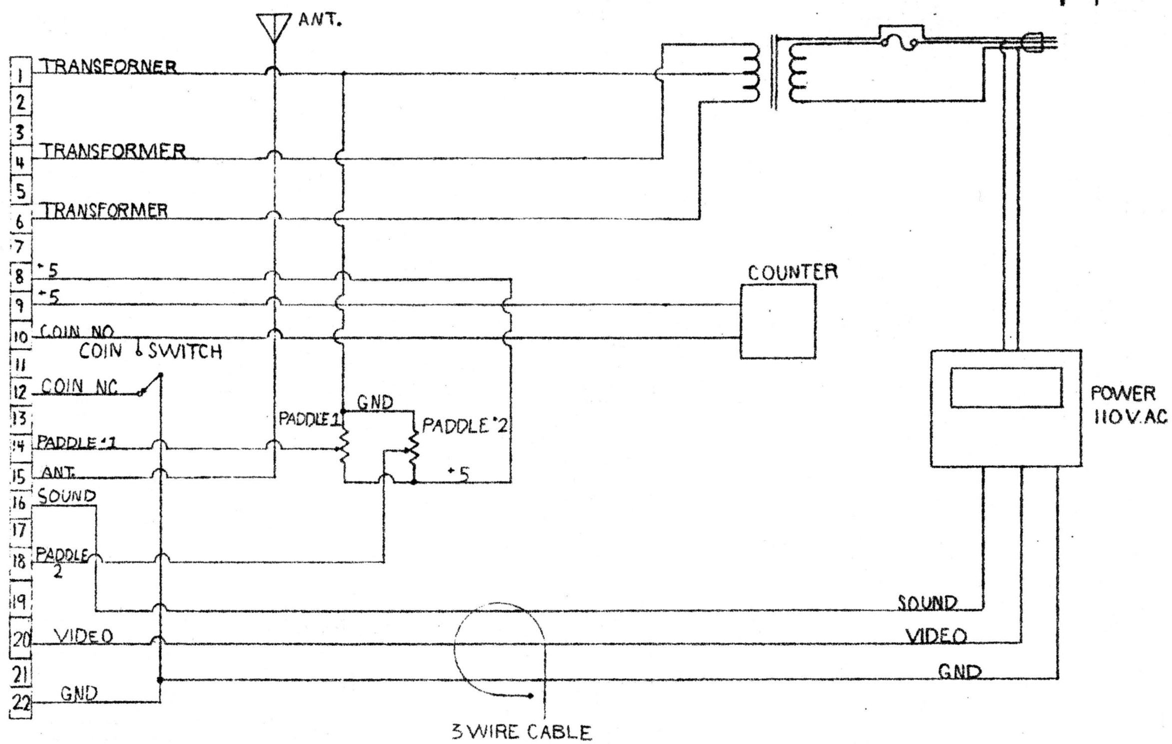
1. 1 piece of 20 A.W.G. sire
2. 1 ¼ Carbon Resistor 4.7K ±10%
   Atari Part No. 10-0472
3. 2 Mouser IC clips 1-Red, 1-Black
   Mouser Part No. Red 13IC 301
   Mouser Part No. Black 13IC 302

STEPS

1. Bend 4.7K Resistor
2. Solder one of the resistors to the Red Mouser IC Clip and solder the other end to the 20 A.W.G. wire.
3. Solder the other end of the 20 A.W.G. wire to the black Mouser IC clip.


PONG
SYZYZY
E
LM309K
470UF
8000 UF
A001433
REV E

REVISIONS				
SYM	DESCRIPTION	INITIALS and DATE: DRFTG	CHECK	ENGRG
G	REDRAWN	TM		



INTERPRET THIS DRAWING PER USASI Y14.5	
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON: FRACTIONS = ±1/16 .x = ±.1 ANGLES = ±1° .xx = ±.03 SURFACE FINISH ✓ .xxx = ±.010	
MATERIAL:	
DRAWN BY T.J.M.	DATE 05-16-74
CHECKED	
DESIGN ENGINEER	
PROJECT ENGINEER	
DOCUMENT CONTROL	
APPROVED	

ATARI INCORPORATED
14600 Winchester Boulevard
Los Gatos, California 95030

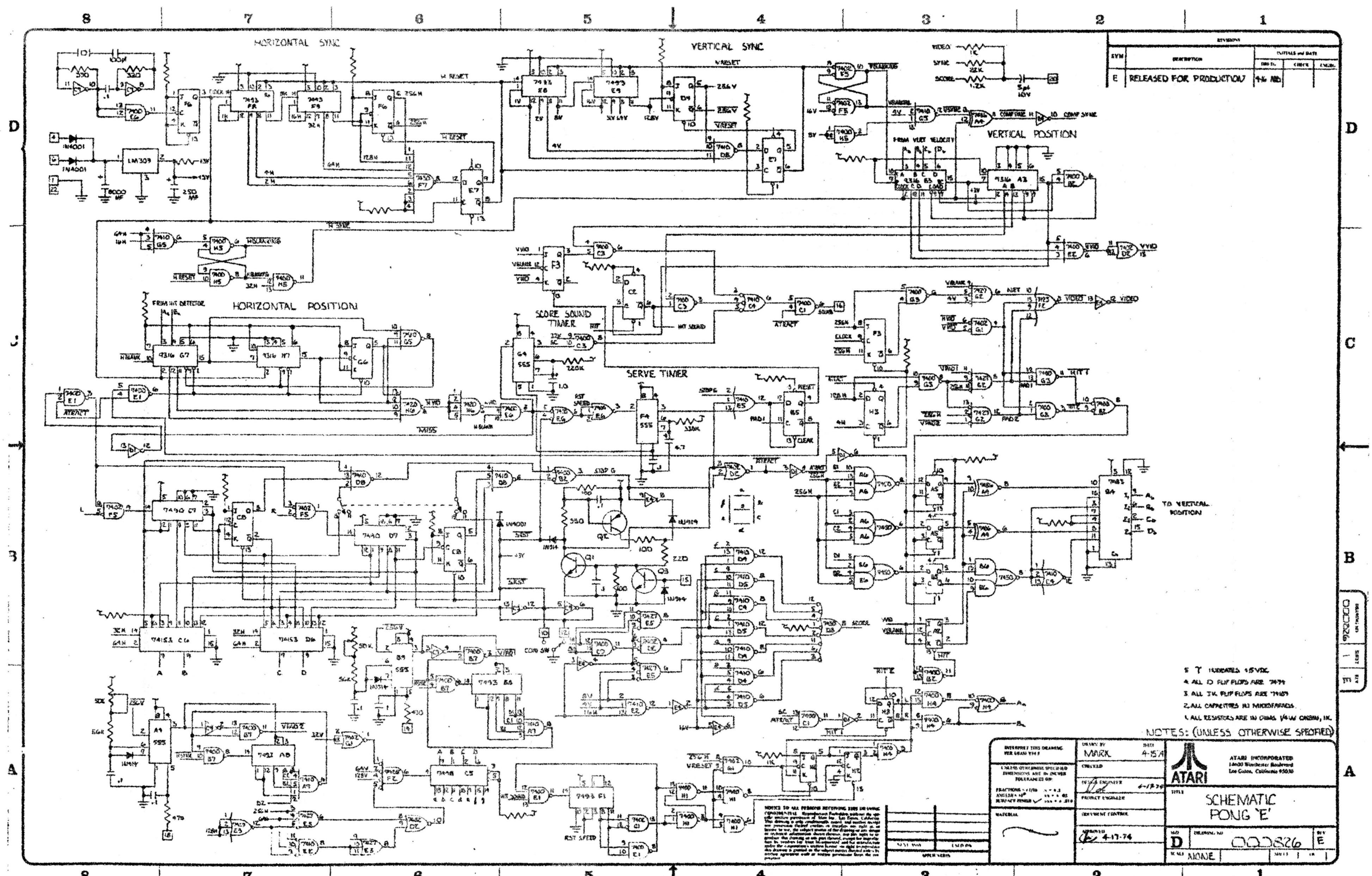
TITLE: PONG WIRE HARNESS

SIZE: C | DRAWING NO. 000753 | REV G

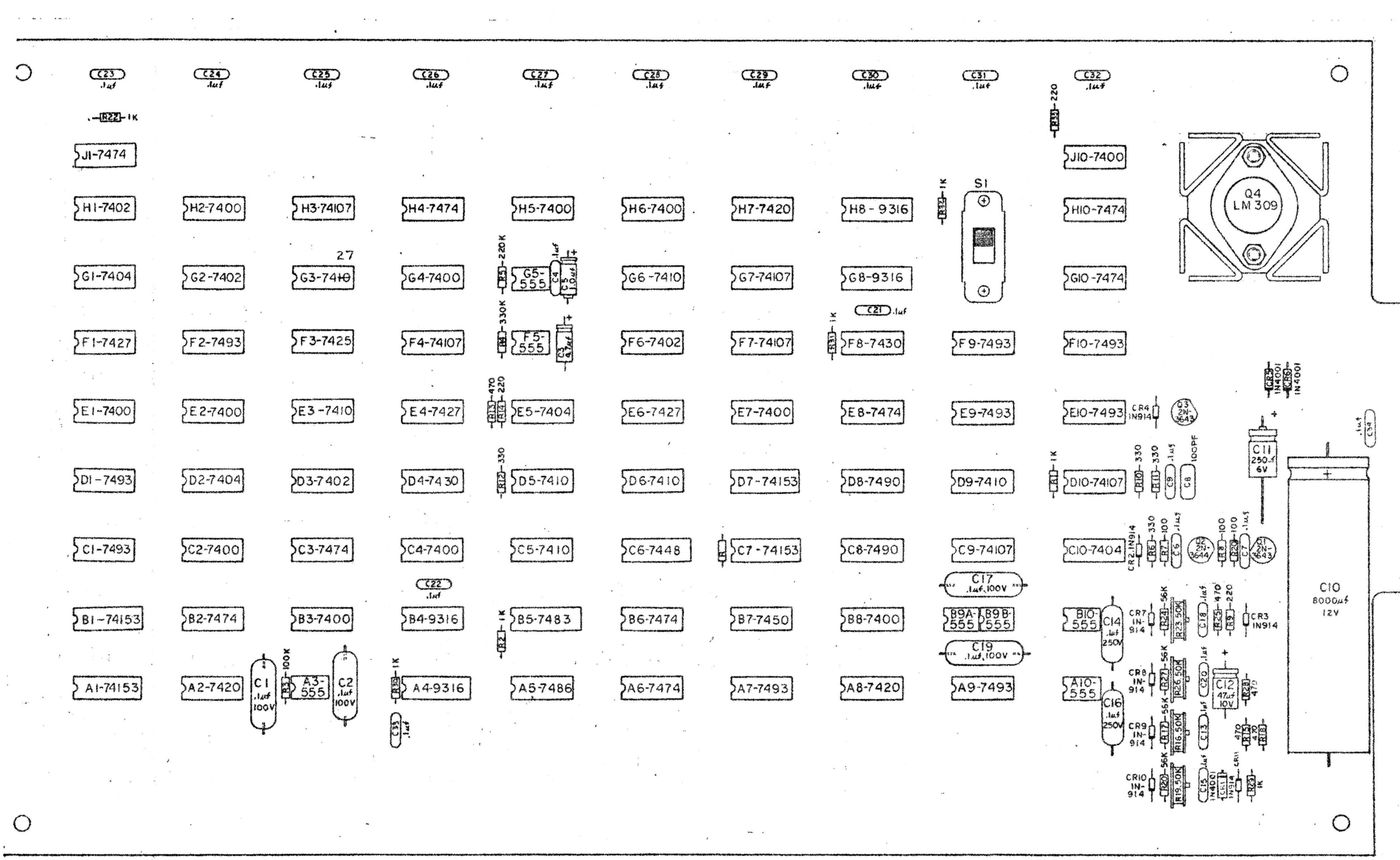
SCALE | SHEET 1 OF 1

NEXT ASSY	USED ON
	PONG
APPLICATION	

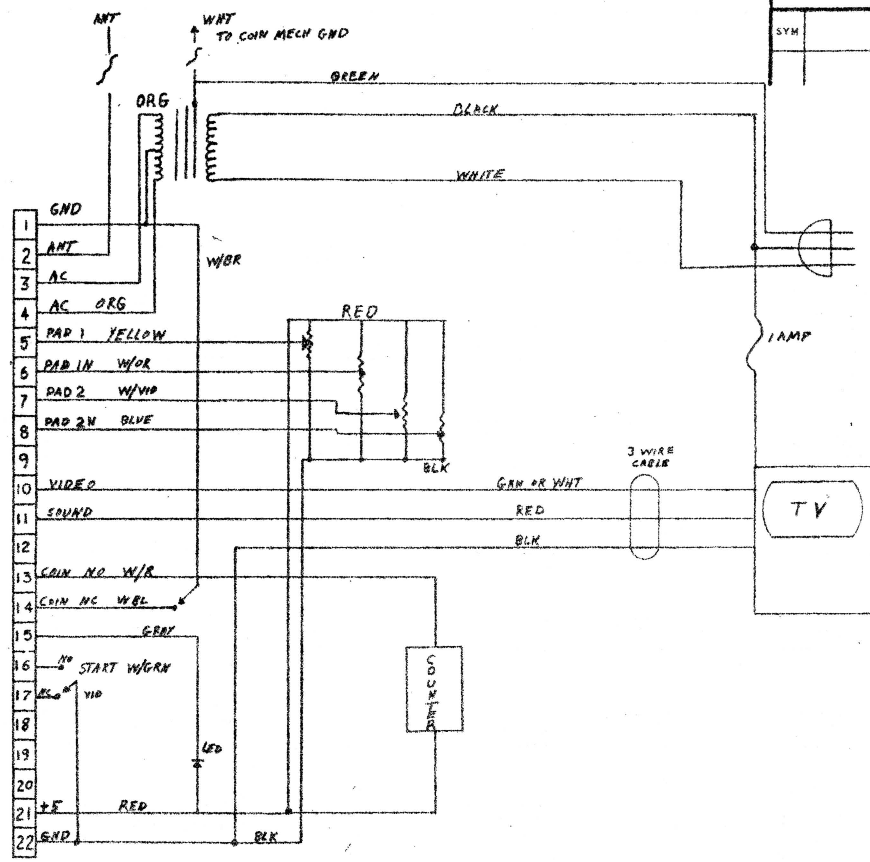
DRAWING NO. 000753 | SHEET 1 | REV



HORIZONTAL SYNC
VERTICAL SYNC
VERTICAL POSITION
HORIZONTAL POSITION
SCORE SOUND TIMER
SERVE TIMER
TO VERTICAL POSITION
REVISIONS
E RELEASED FOR PRODUCTION
NOTES: (UNLESS OTHERWISE SPECIFIED)
1. ALL RESISTORS ARE IN OHMS 1/4W CARBON, 1K.
2. ALL CAPACITORS IN MICROFARADS.
3. ALL JK FLIP FLOPS ARE 74107
4. ALL D FLIP FLOPS ARE 7474
5. ⊤ INDICATES +5VDC.
ATARI
ATARI INCORPORATED
14600 Winchester Boulevard
Los Gatos, California 95030
SCHEMATIC
PONG 'E'
DRAWN BY MARK 4-15-74
D
003826
E
SCALE NONE



PONG DOUBLES "F"



SYM	DESCRIPTION	DRFTG	CHECK	ENGRG

REVISIONS — INITIALS and DATE

NOTICE TO ALL PERSONS RECEIVING THIS DRAWING
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NEXT ASSY | USED ON
APPLICATION

INTERPRET THIS DRAWING PER USASI Y14.5

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON:
FRACTIONS ± 1/16 .x ± .1
ANGLES ± 1° .xx ± .03
SURFACE FINISH ✓ .xxx ± .010

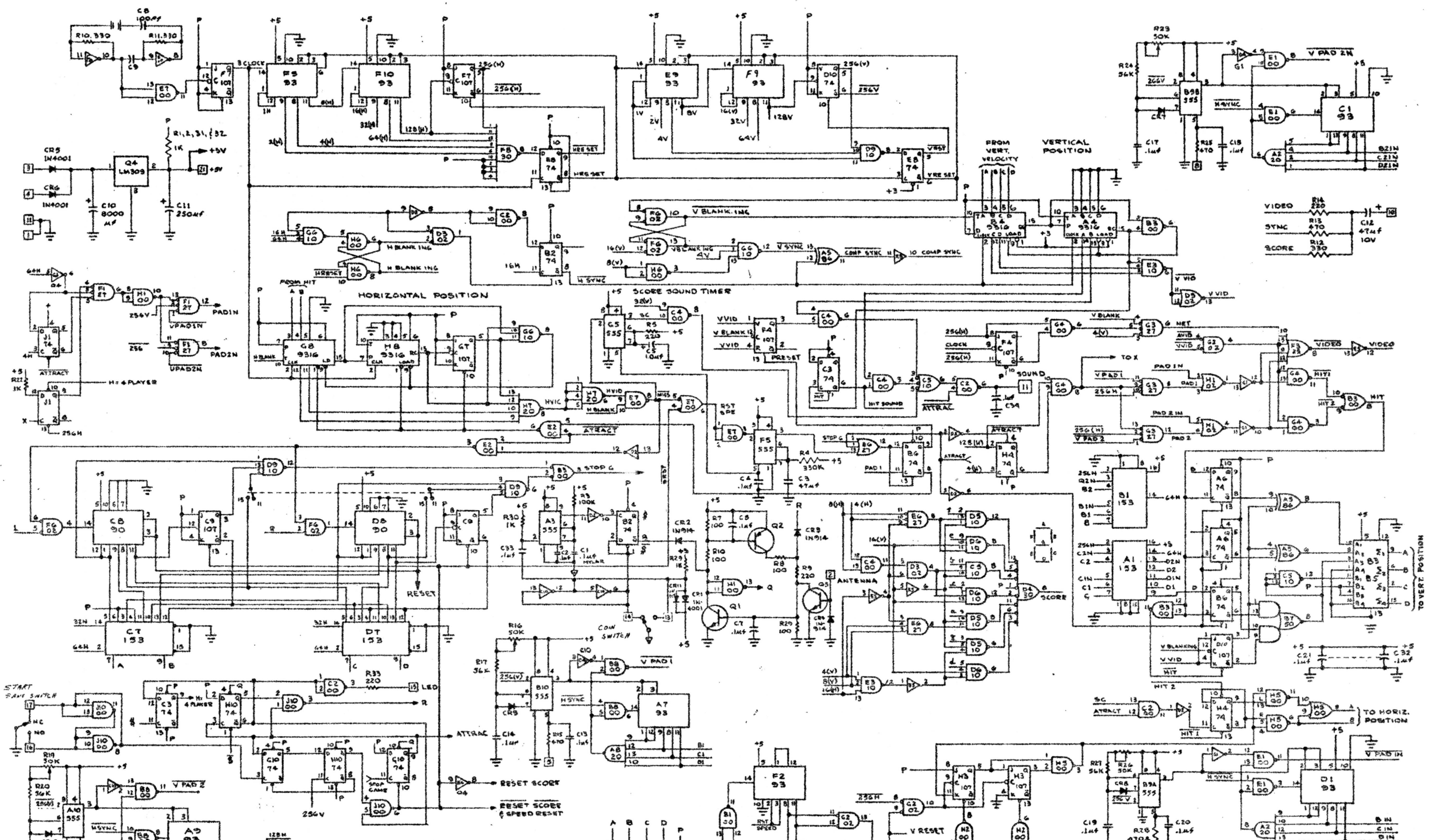
MATERIAL:

DRAWN BY M. JONES DATE 10-14-74
CHECKED
DESIGN ENGINEER
PROJECT ENGINEER
DOCUMENT CONTROL
APPROVED

ATARI INCORPORATED
14600 Winchester Boulevard
Los Gatos, California 95030

TITLE
PONG DBL'S HARNESS

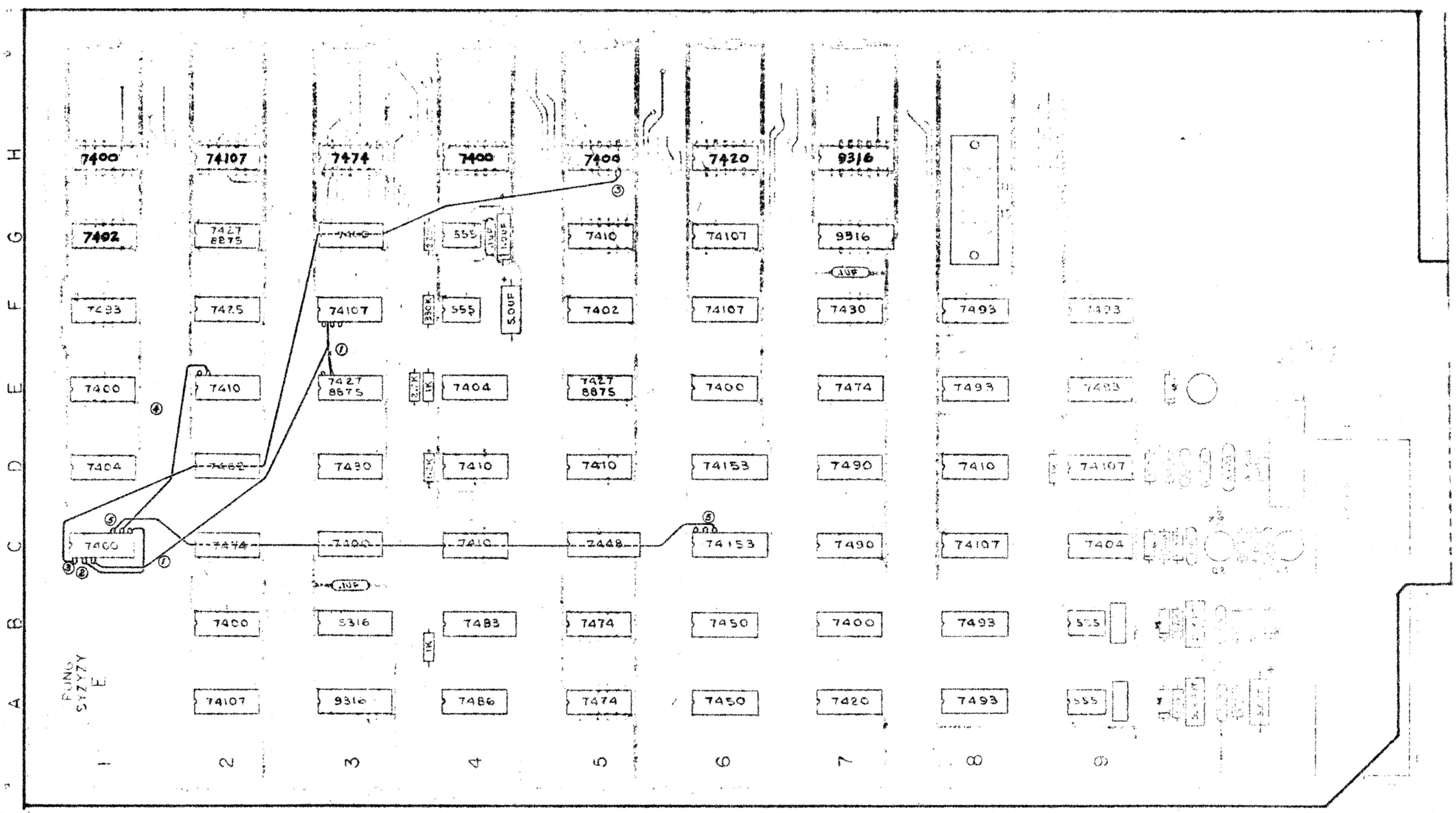
SIZE C | DRAWING NO. 000783 | REV D
SCALE — | SHEET 1 OF 1



Atari Inc 14600 Winchester Blvd
Los Gatos, CA., 95030
408-374-2440
Rev F

Schematic Pong Doubles

DRN: PCD 10-17-73 APP:
SH 1 OF 1



NOTES: UNLESS OTHERWISE SPECIFIED

THE OPERATIONS DEFINED BELOW INVOLVE THE FABRICATION OF SUPERPONG CIRCUIT BOARD BY MODIFICATION OF "E" REVISION, PONG BOARD, (VP101).

1. IN AREA BETWEEN CHIP E3 & F3 LOCATE TRACE FROM E3 PIN 13 & CUT TRACE NEAR E3, AT POINT "X" AS SHOWN. ABOVE CUT, SOLDER WIRE TO TERMINATED TRACE (NOT CONNECTED TO E3), & TERMINATE FREE END OF THIS WIRE AT C1, PIN 3.

2. ATTACH JUMPER WIRE FROM C1, PIN 2, TO C1, PIN 8, AS SHOWN.

3. ATTACH JUMPER WIRE FROM C1, PIN 1, TO H5, PING, AS SHOWN.

4. ATTACH JUMPER WIRE FROM C1, PIN 9, TO E2, PIN 13, AS SHOWN.

5. ATTACH JUMPER WIRE FROM C1, PIN 10, TO C6, PIN 14, AS SHOWN.

NOTE: ALL JUMPER WIRE USED IN THE ABOVE FIVE STEPS SHALL BE 30 AWG WIRE, KYNAR INSULATED, OR EQUIV.
ALL INTERCONNECTING JUMPERS SHALL BE ROUTED AS SHOWN IN THE ABOVE DIAGRAM.

LTR	DESCRIPTION	APPR
A	PRE-PROD REL.	

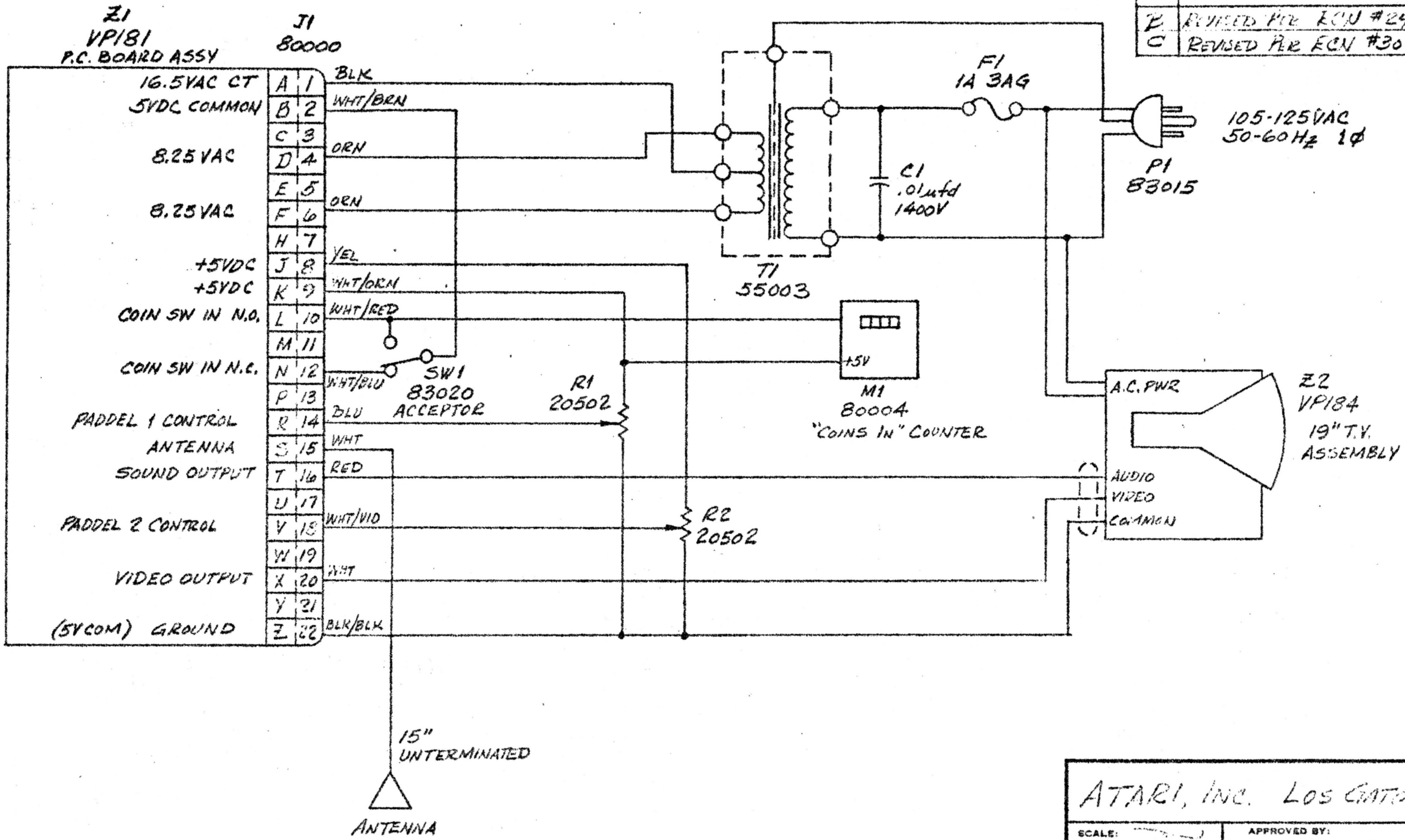
ATARI, INC LOS GATOS, CALIF

FABRICATION DWG,
PRINTED CIRCUIT BOARD

BY: R.C. WAYNE
DATE: JAN 5, 1974

SUPERPONG, VP181 DWG Nº 000423 REV. "A"

REV	DESCRIPTION	APRV
A	PRE-PROD REL	
B	REVISED PER ECN #24	
C	REVISED PER ECN #30	



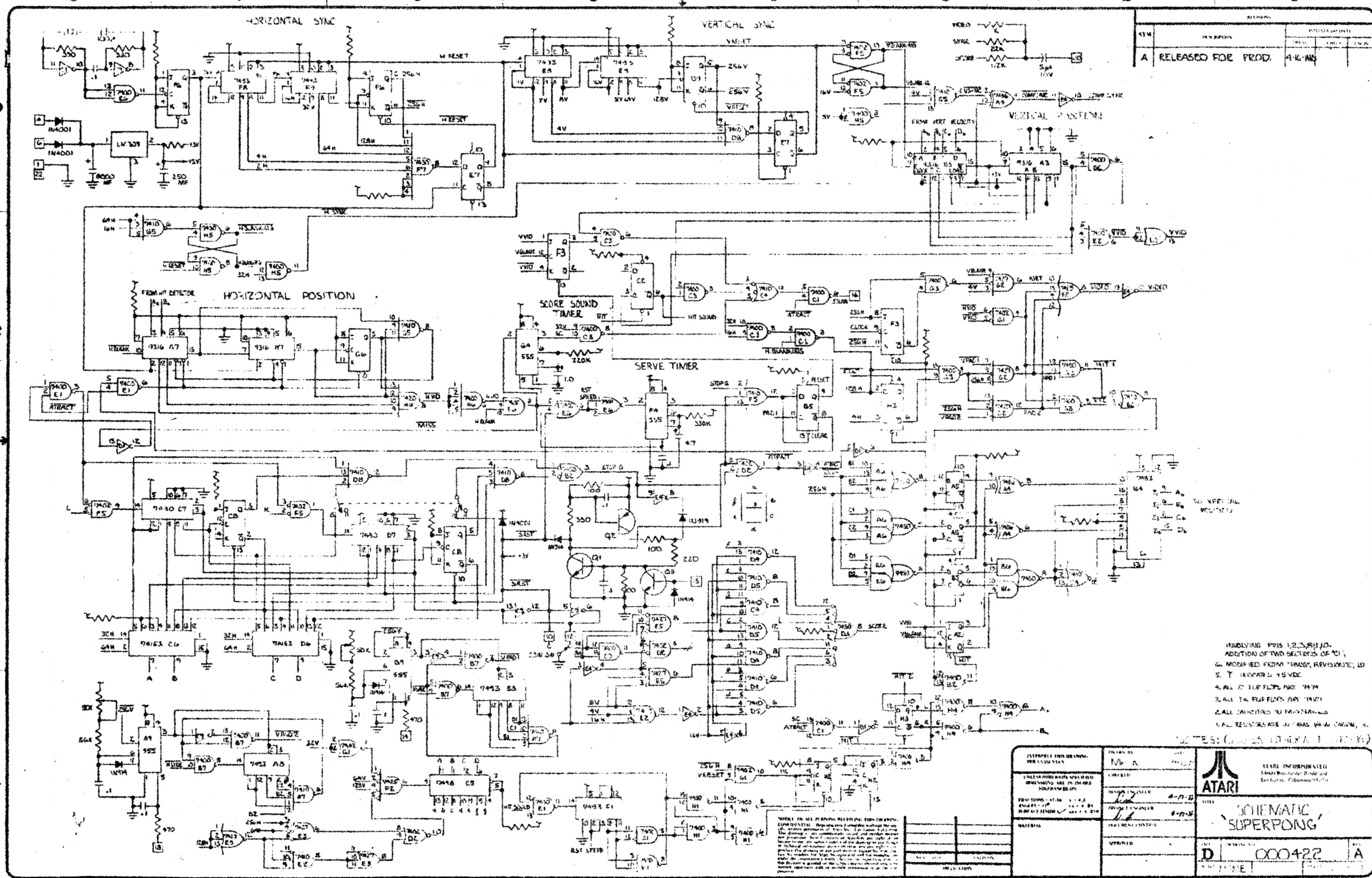
ATARI, INC. LOS GATOS, CALIF

SCALE:	APPROVED BY:	DRAWN BY
DATE: JUNE 1974		REVISED C

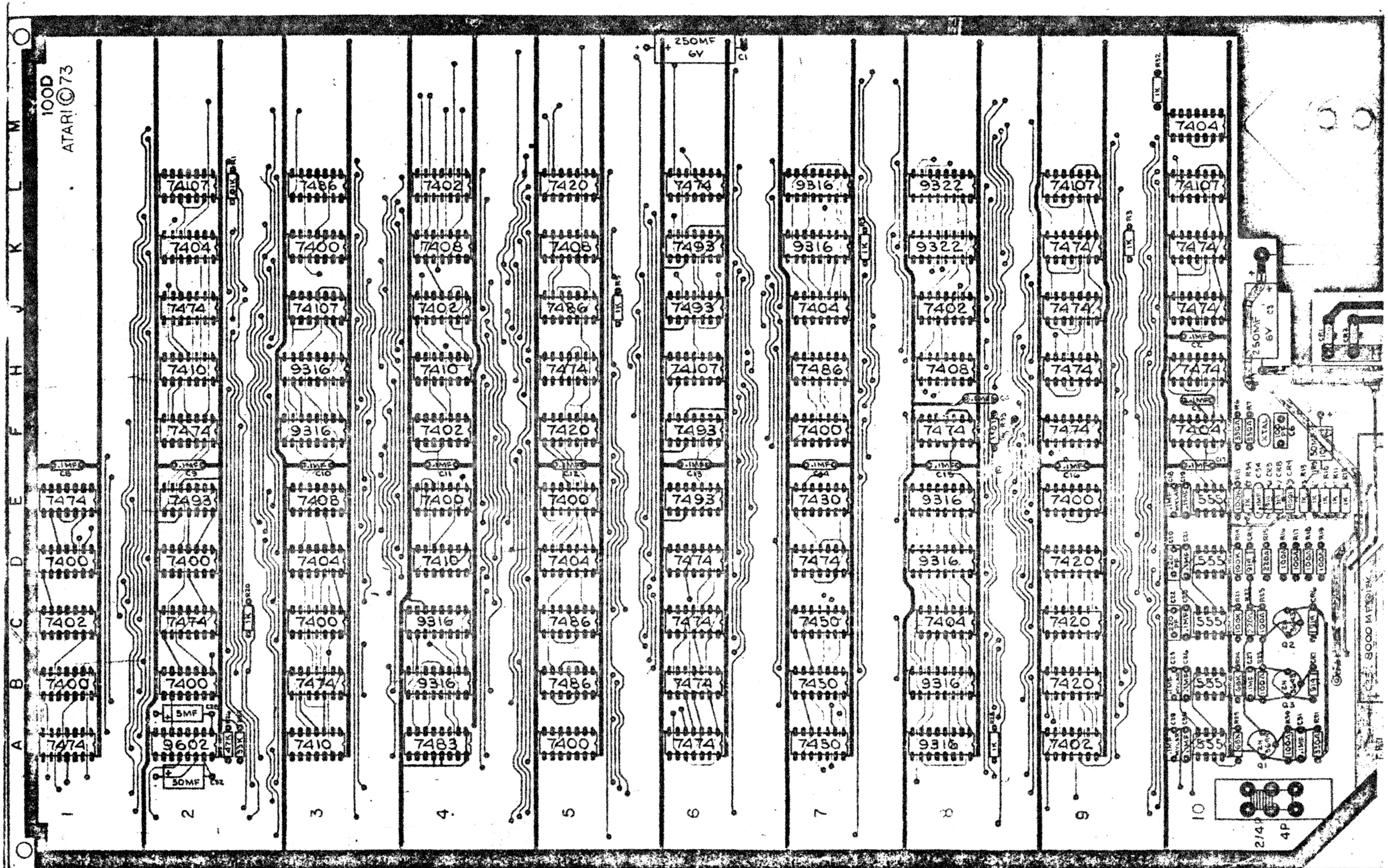
ENCLOSURE WIRING, SCHEMATIC DIAGRAM

SUPER PONG — DRAWING NUMBER 000419

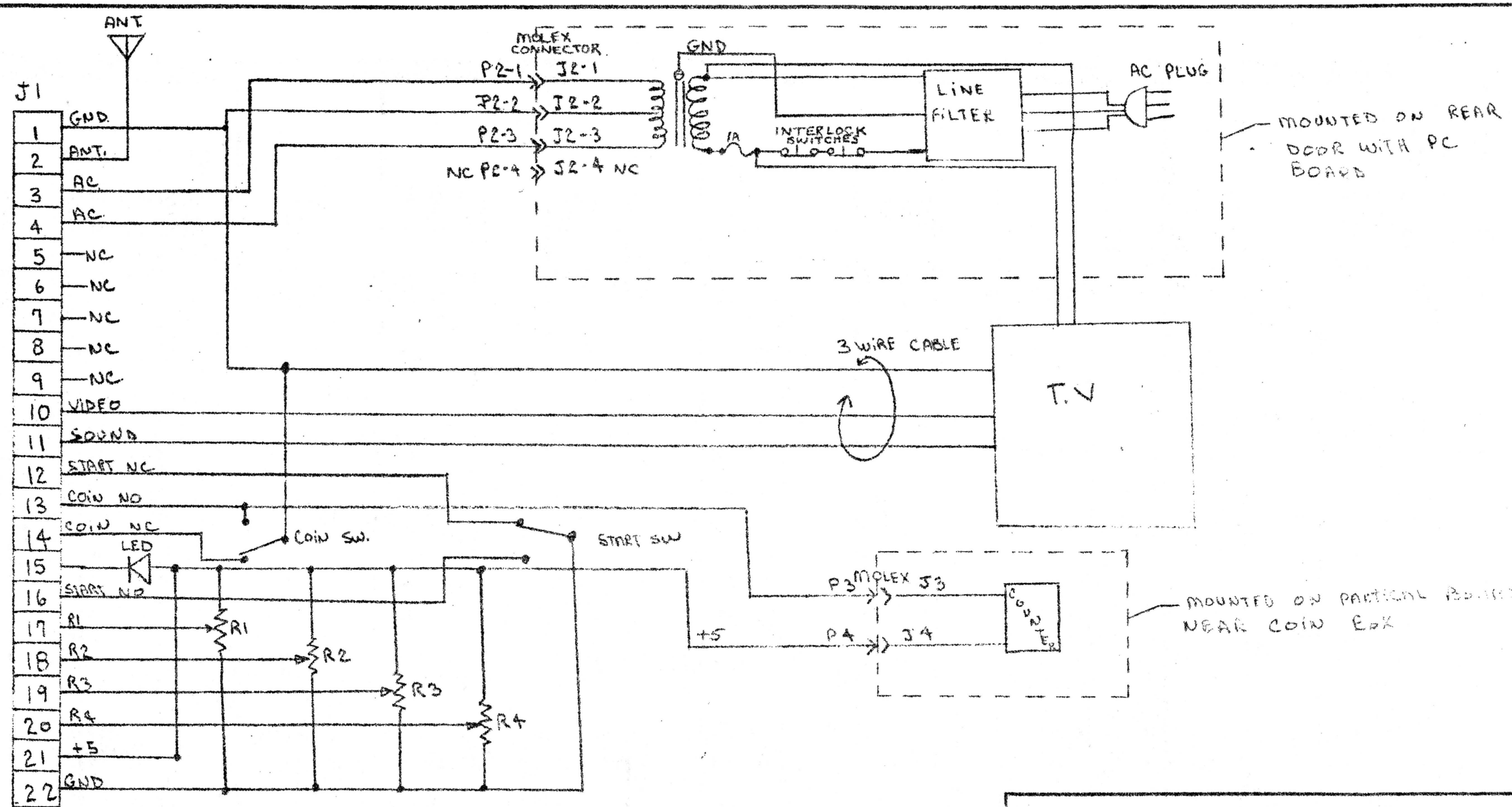
11X17 PRINTED ON NO. 1000H CLEARPRINT



HORIZONTAL SYNC
VERTICAL SYNC
VERTICAL POSITION
HORIZONTAL POSITION
SCORE SOUND TIMER
SERVE TIMER
A RELEASED FOR PROD.
ATARI
SCHEMATIC 'SUPERPONG'
D 000422 A

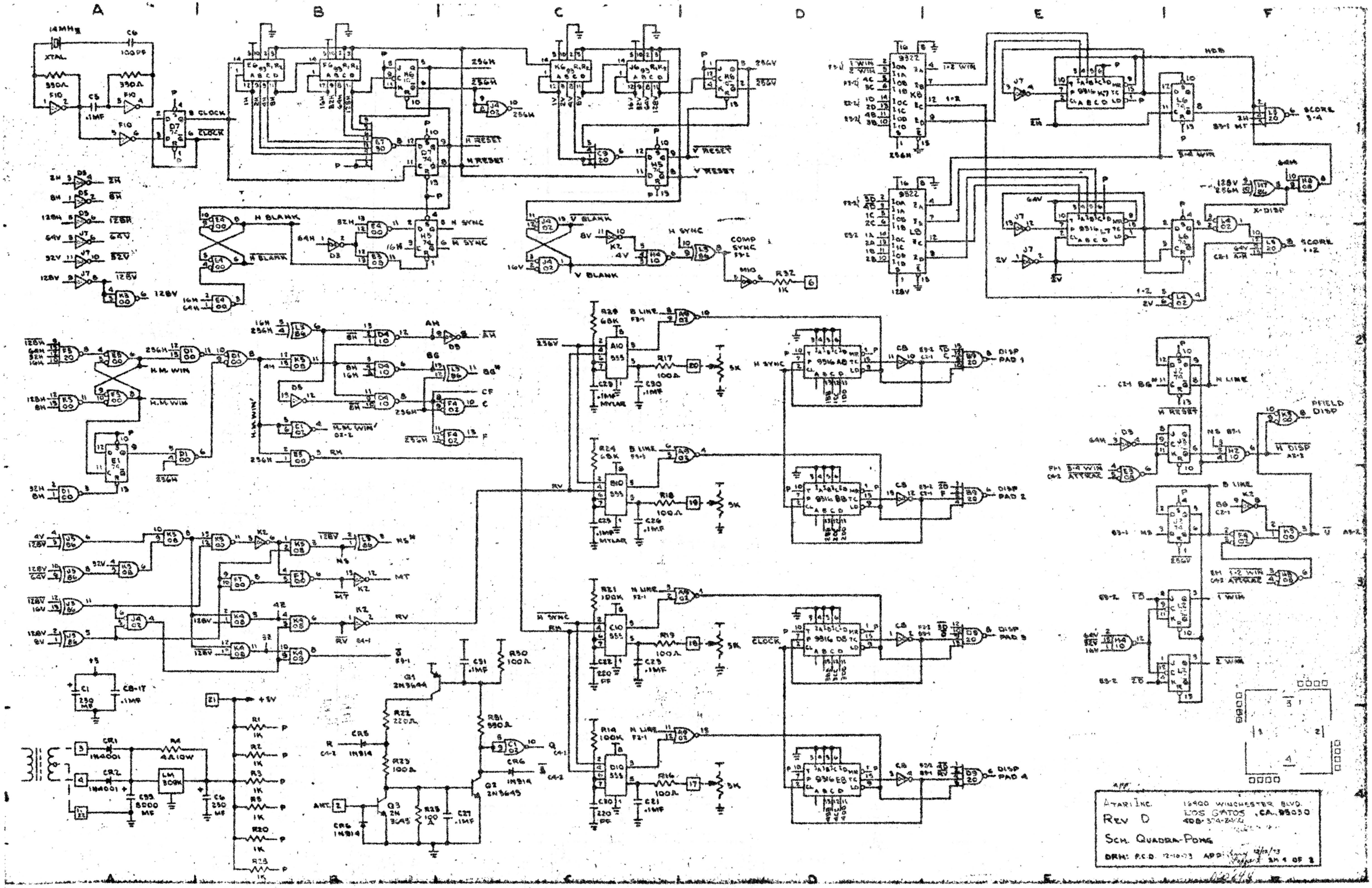


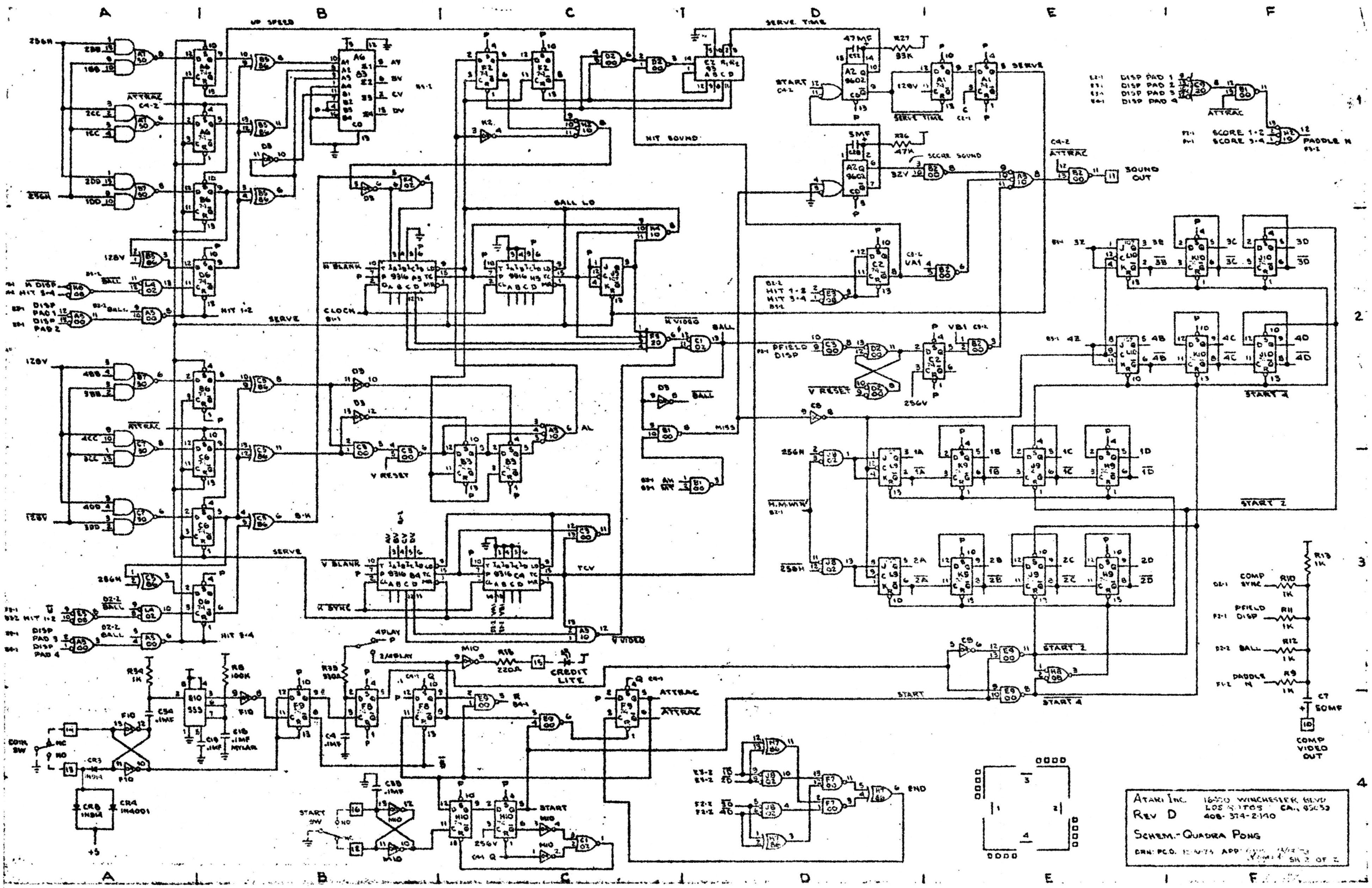
QUAD D 12-10-73

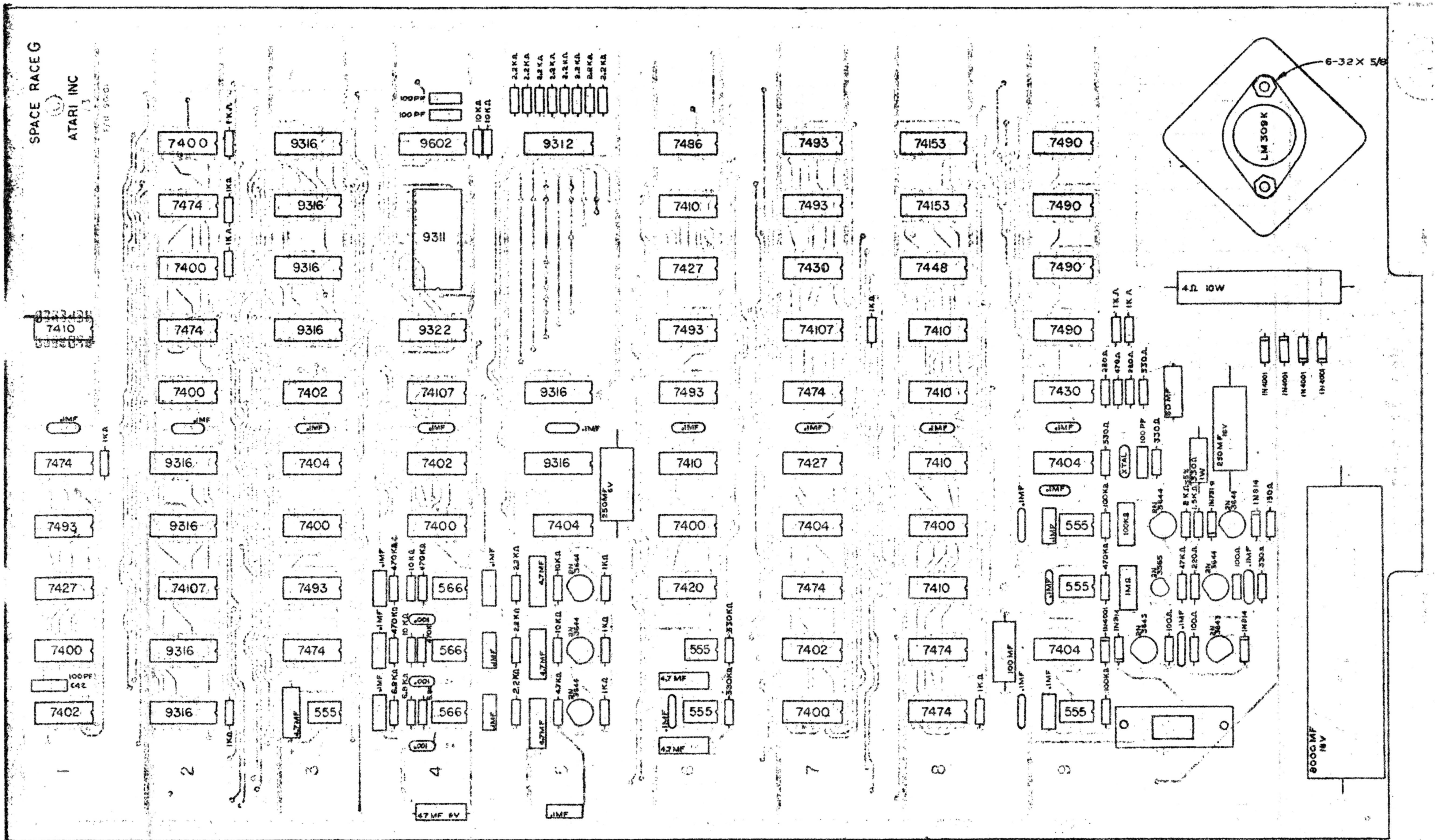


QUADRAPONG HARNESS ELEC. ASSE		
SCALE:	APPROVED BY:	DRAWN BY
DATE: 12/12/73	12/13/73	REVISED
		DRAWING NUMBER

11X17 PRINTED ON NO. 1000H CLEARPRINT


ATARI INC.
16400 WINCHESTER BLVD.
LOS GATOS, CA. 95030
408-374-2440
REV D
SCH. QUADRA-PONG
DRN: P.C.D. 12-10-73 APP:
SH 1 OF 2

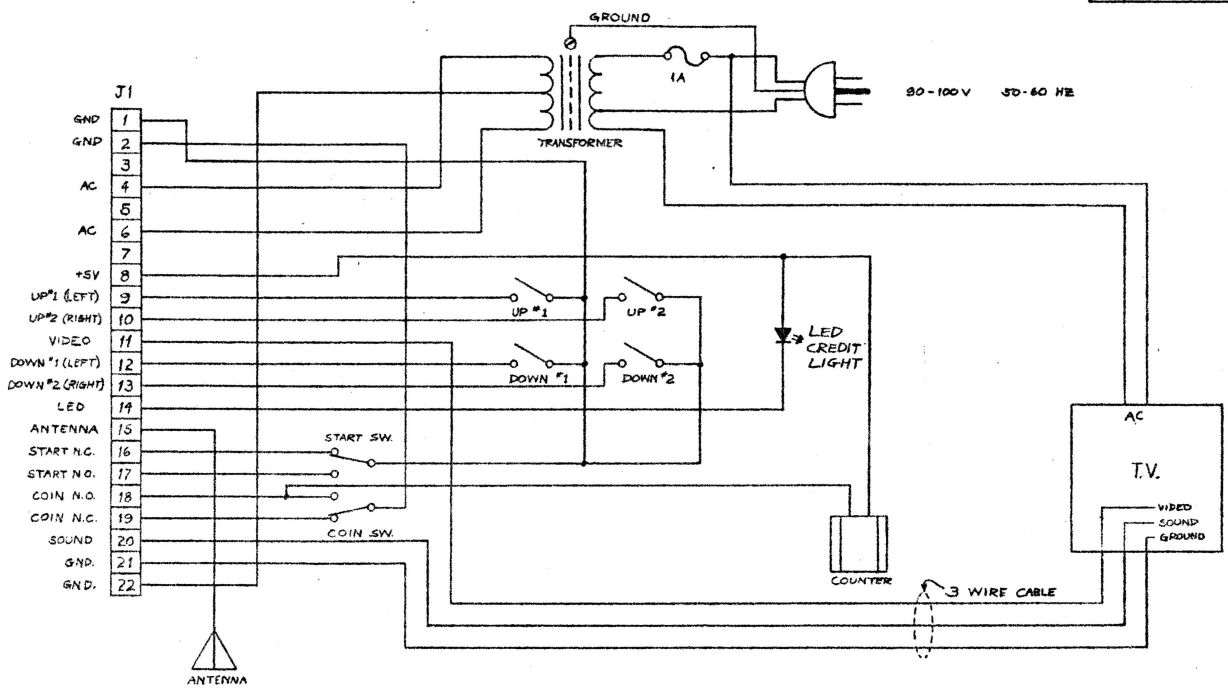

Atari Inc. 16600 Winchester Blvd
Los Gatos Ca., 95032
408-374-2440
Rev D
Schem.-Quadra Pong
DRN: PC.O. 12-4-74 APP 12/12/73 SH 2 OF 2



* USE CR5 OR R28, R29, & Q2

STUFFING for SR
000803

REVISIONS				
SYM	DESCRIPTION	INITIALS and DATE		
		DRFTG	CHECK	ENGRG
A	REL. TO PROD. REDRAWN	5/16/74	D.L.	
B	REV. PER ECN 517	6/24/74	D.L.	WMD 6/25



NOTES:

1. ALL SWITCHES SHOWN IN THEIR NORMAL POSITIONS

NEXT ASSY	USED ON
	SPACE RACE
APPLICATION	

INTERPRET THIS DRAWING PER USASI Y14.5

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON:
FRACTIONS = ±1/16 .x = ±.1
ANGLES = ±1° .xx = ± .03
SURFACE FINISH ✓ .xxx = ± .010

MATERIAL:

DRAWN BY T. Fowlks DATE 5/16/74
CHECKED
DESIGN ENGINEER
PROJECT ENGINEER D. Lang
DOCUMENT CONTROL
APPROVED [illegible] 6/25/74

ATARI

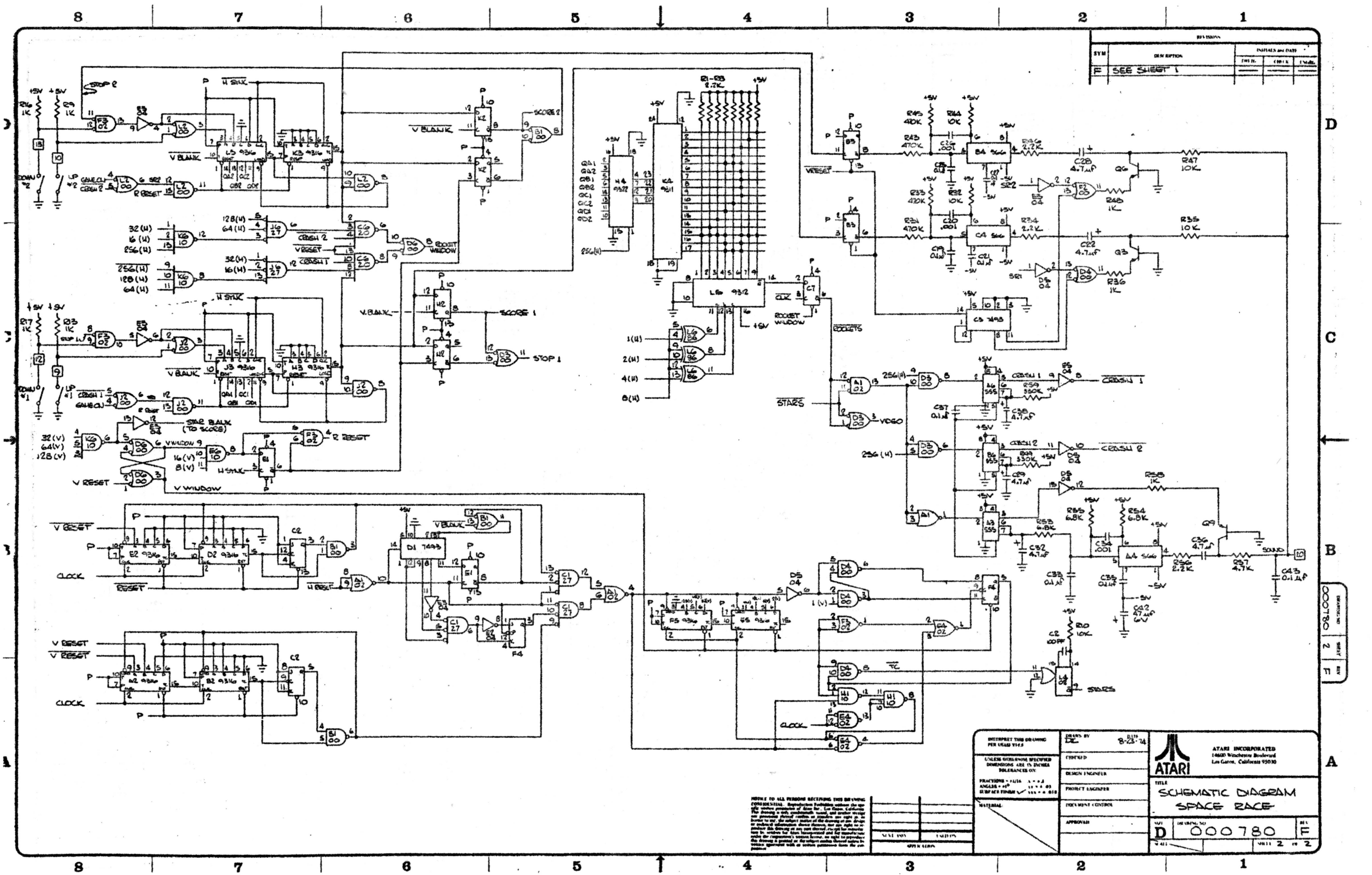
ATARI INCORPORATED
14600 Winchester Boulevard
Los Gatos, California 95030

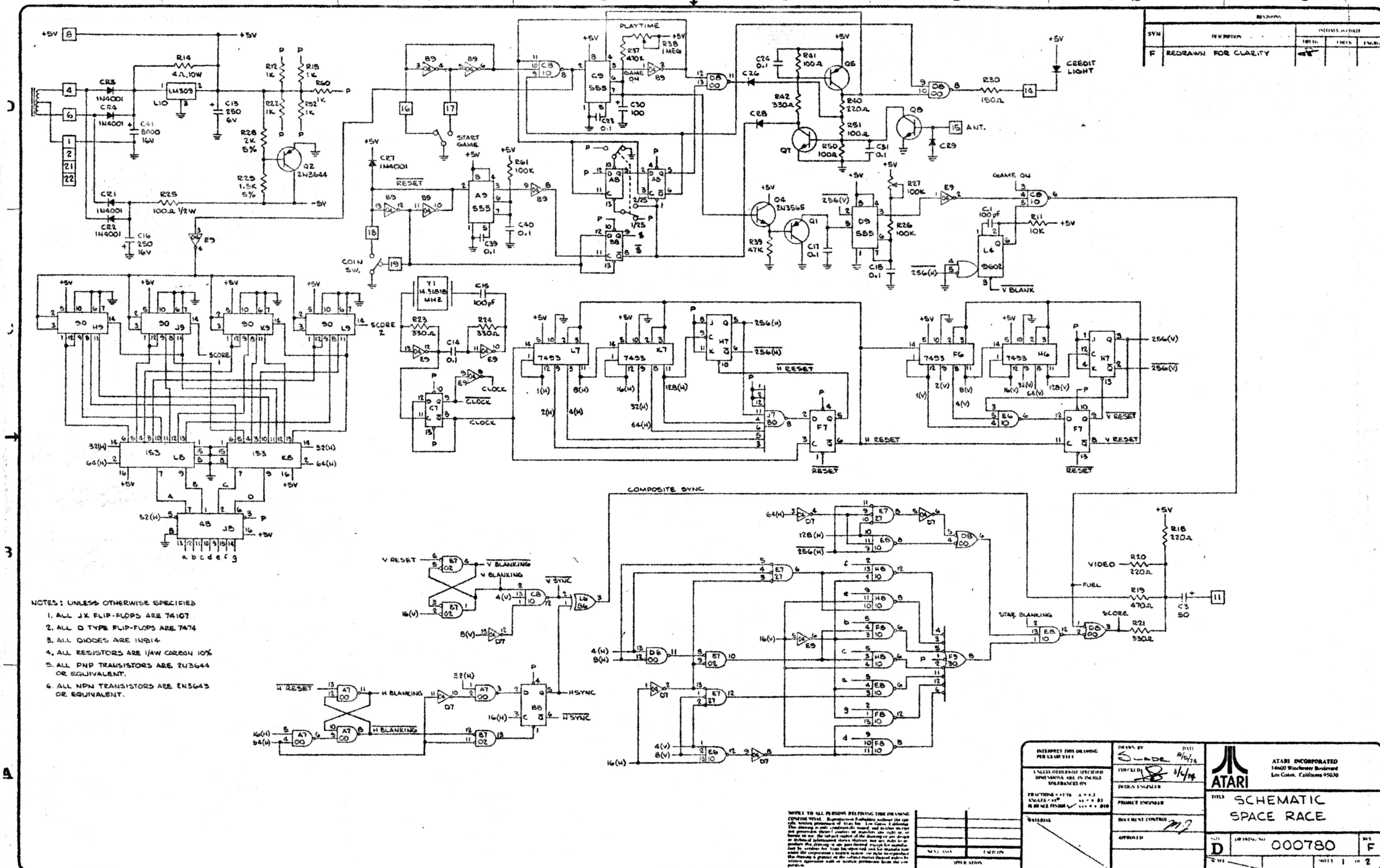
TITLE WIRING HARNESS S.R.

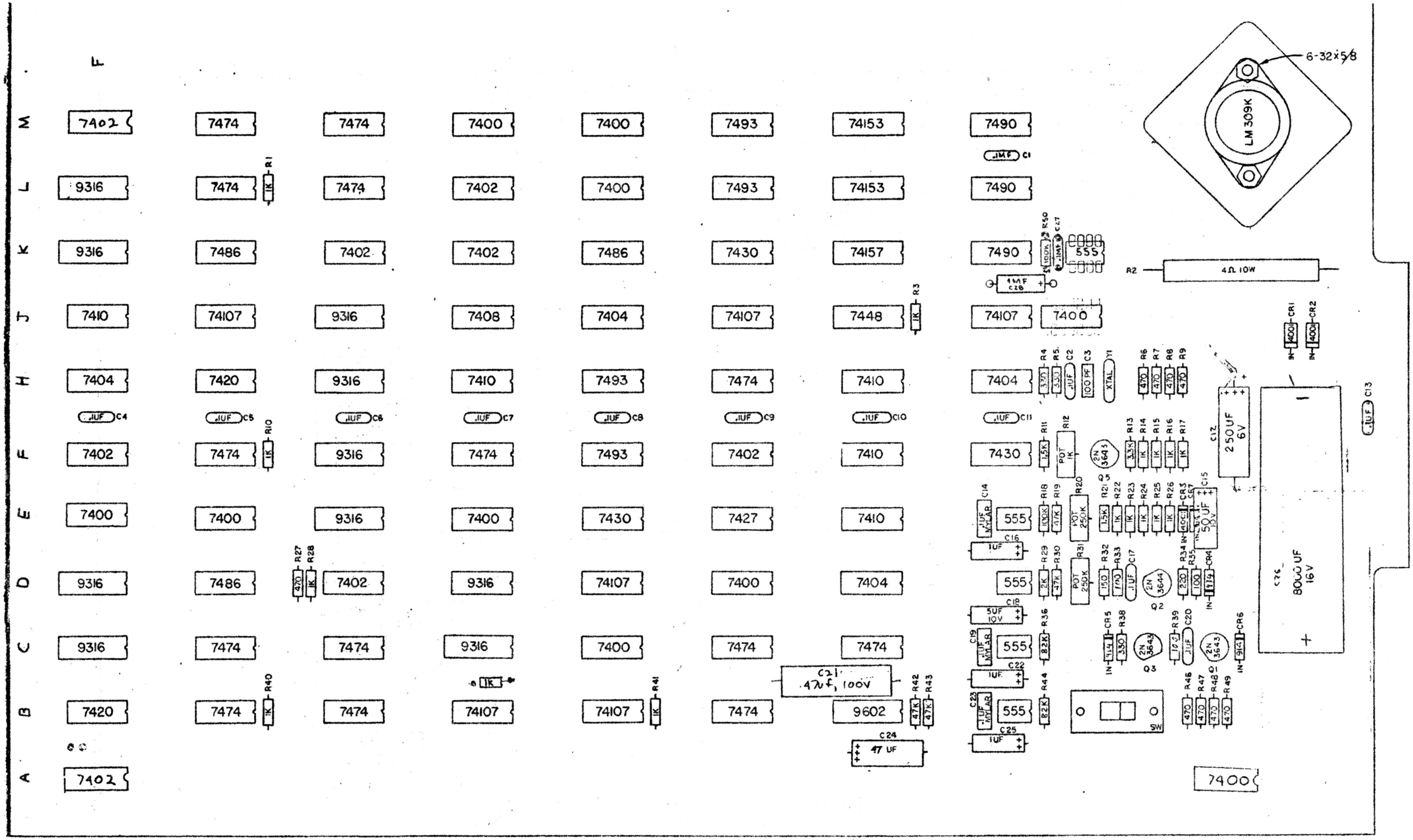
SIZE C DRAWING NO. 000771 REV B

SCALE NONE SHEET 1 OF 1

DRAWING NO. 000771 SHEET 1/1 REV B

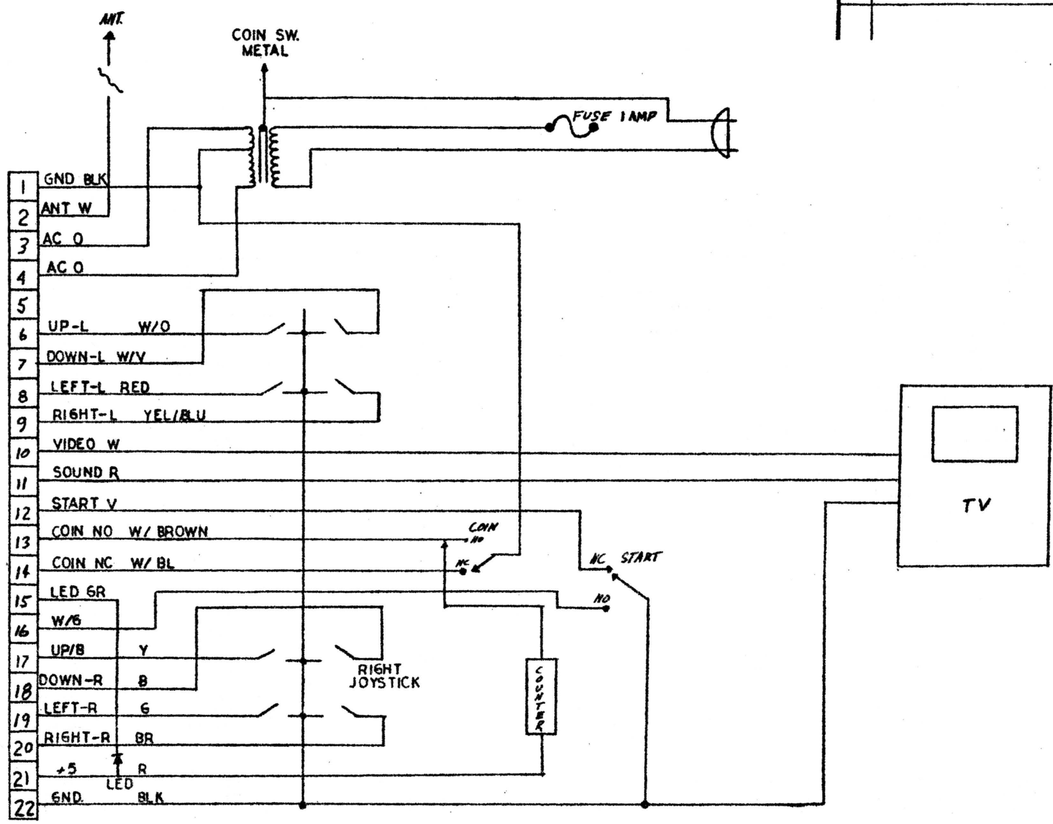

SEE SHEET 1
ATARI INCORPORATED
14600 Winchester Boulevard
Los Gatos, California 95030
SCHEMATIC DIAGRAM
SPACE RACE
D 000780 F
SHEET 2 OF 2
8-23-74


NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL JK FLIP-FLOPS ARE 74107
2. ALL D TYPE FLIP-FLOPS ARE 7474
3. ALL DIODES ARE 1N914
4. ALL RESISTORS ARE 1/4W CARBON 10%
5. ALL PNP TRANSISTORS ARE 2N3644 OR EQUIVALENT.
6. ALL NPN TRANSISTORS ARE 2N3643 OR EQUIVALENT.
F REDRAWN FOR CLARITY
ATARI INCORPORATED
14600 Winchester Boulevard
Los Gatos, California 95030
SCHEMATIC
SPACE RACE
D 000780 F
SHEET 1 OF 2
COMPOSITE SYNC
CREDIT LIGHT
PLAYTIME
START GAME
COIN SW.
SCORE 1
SCORE 2
VIDEO
FUEL
STAR BLANKING
GAME ON



SYZYGY 2962 SCOTT BLVD.
SANTA CLARA, CA., 95050
415-247-4825
REV F
ASSY. --- GOTCHA
DRWN. PC DESIGN 7-25-73

REVISIONS				
SYM	DESCRIPTION	INITIALS and DATE		
		DRFTG	CHECK	ENGRG



NEXT ASSY	USED ON
APPLICATION	

INTERPRET THIS DRAWING PER USASI Y14.5

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON:
FRACTIONS = ±1/16 .x = ±.1
ANGLES = ±1° .xx = ±.03
SURFACE FINISH ✓ .xxx = ±.010

MATERIAL:

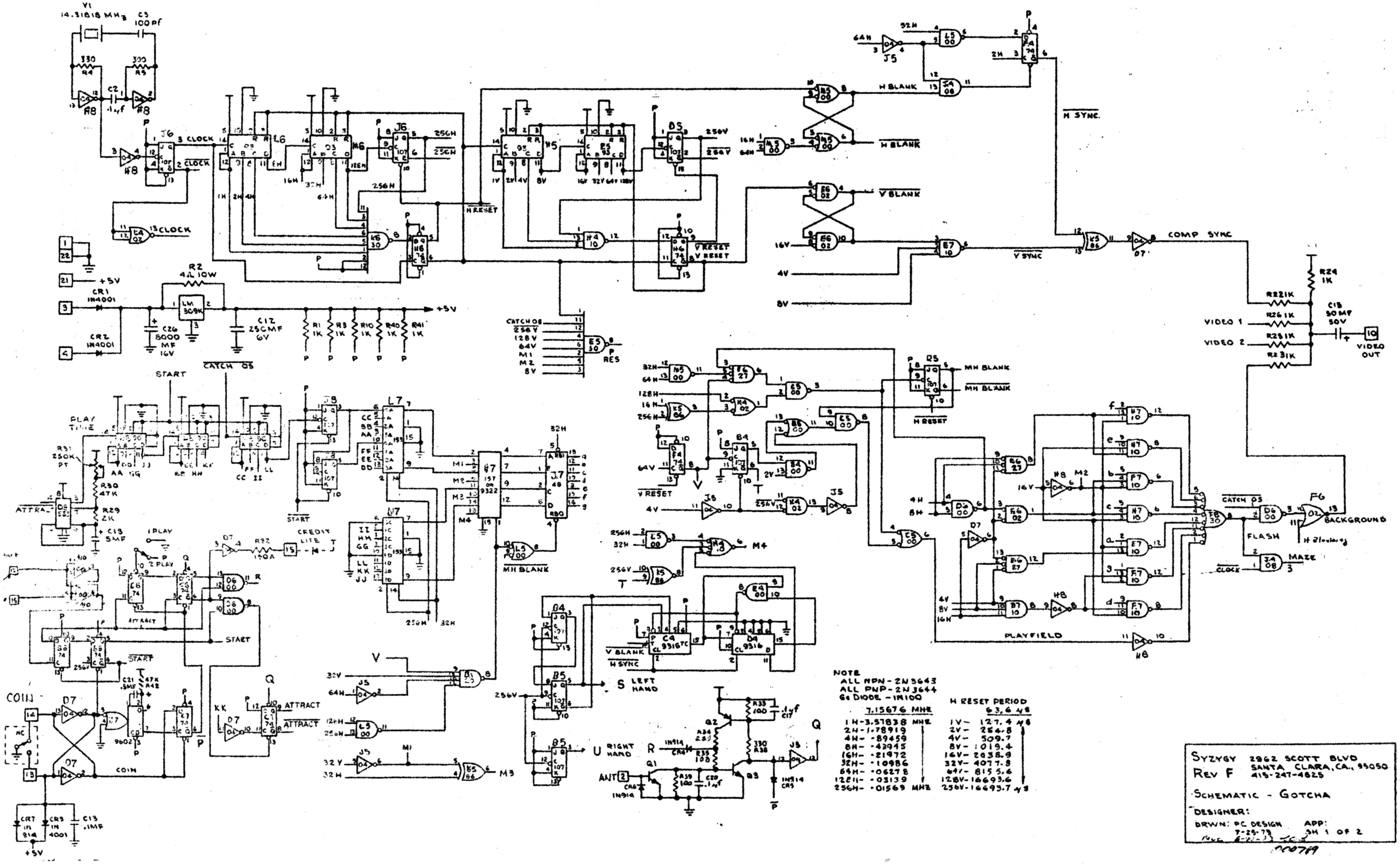
DRAWN BY M. JONES DATE 10-14-74
CHECKED
DESIGN ENGINEER
PROJECT ENGINEER
DOCUMENT CONTROL M.J.
APPROVED

ATARI INCORPORATED
14600 Winchester Boulevard
Los Gatos, California 95030

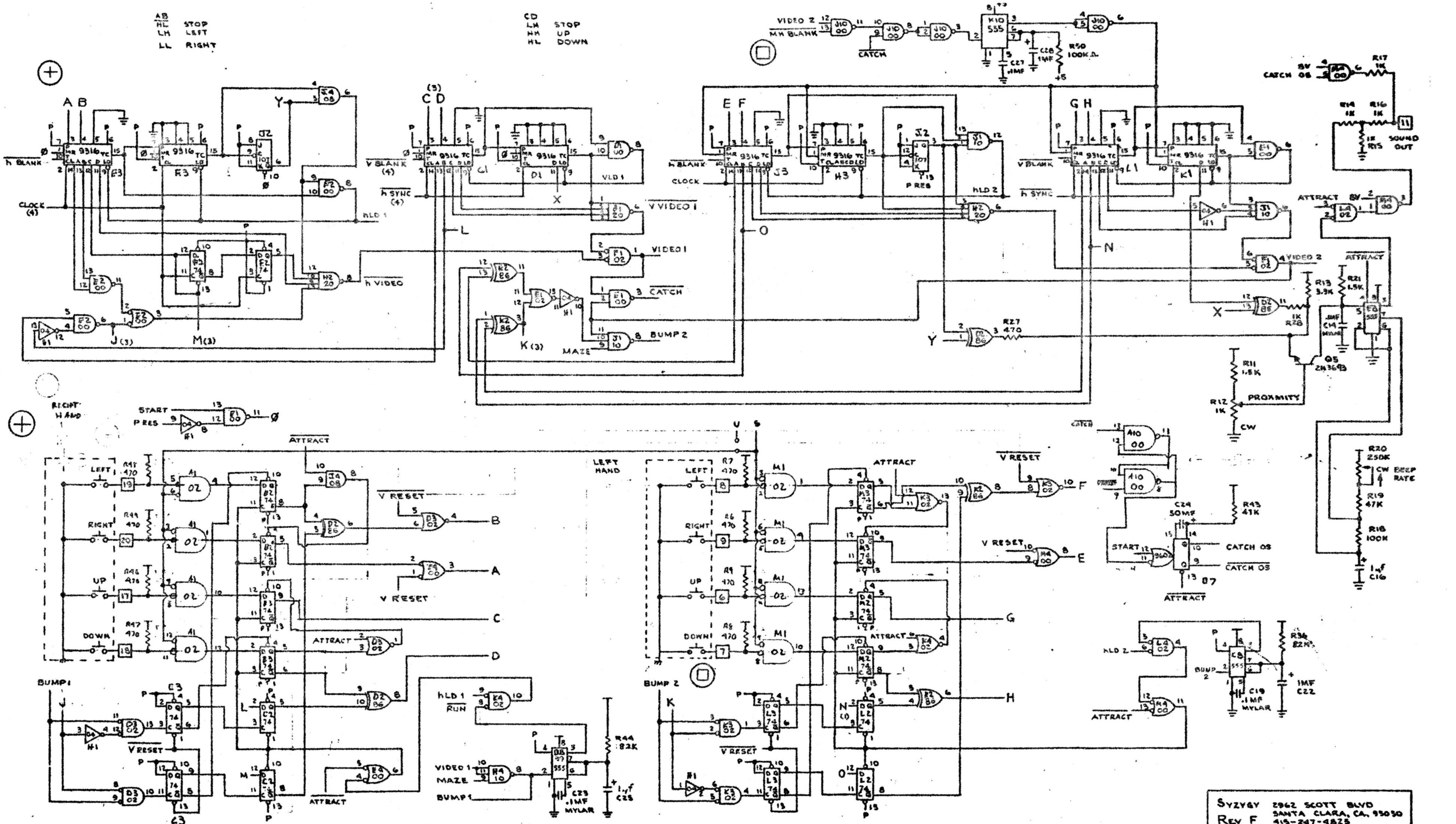
TITLE GOTCHA WIRE HARNESS

SIZE C | DRAWING NO. 000768 | REV C
SCALE — | SHEET 1 OF 1

DRAWING NO. 000768 SHEET 1/1 REV C



NOTE
ALL NPN - 2N3643
ALL PNP - 2N3644
Ge DIODE - 1N100
7.15676 MHz
1H - 3.57838 MHz
2H - 1.78919
4H - .89459
8H - .43945
16H - .21972
32H - .10986
64H - .06278
128H - .03139
256H - .01569 MHz
H RESET PERIOD
63.6 μs
1V - 127.4 μs
2V - 254.8
4V - 509.7
8V - 1019.4
16V - 2038.9
32V - 4077.8
64V - 8155.6
128V - 16693.6
256V - 16693.7 μs
SYZYGY 2962 SCOTT BLVD
SANTA CLARA, CA., 95050
415-247-4825
REV F
SCHEMATIC - GOTCHA
DESIGNER:
DRWN: PC DESIGN
7-25-73
APP:
SH 1 OF 2
COMP SYNC
VIDEO OUT
PLAYFIELD
BACKGROUND
MAZE
FLASH
H SYNC
V SYNC
H BLANK
V BLANK
H RESET
V RESET
CLOCK
START
ATTRACT
CREDIT LITE
COIN
LEFT HAND
RIGHT HAND



Syzygy 2962 Scott Blvd
Santa Clara, CA. 95030
Rev F 415-247-4825

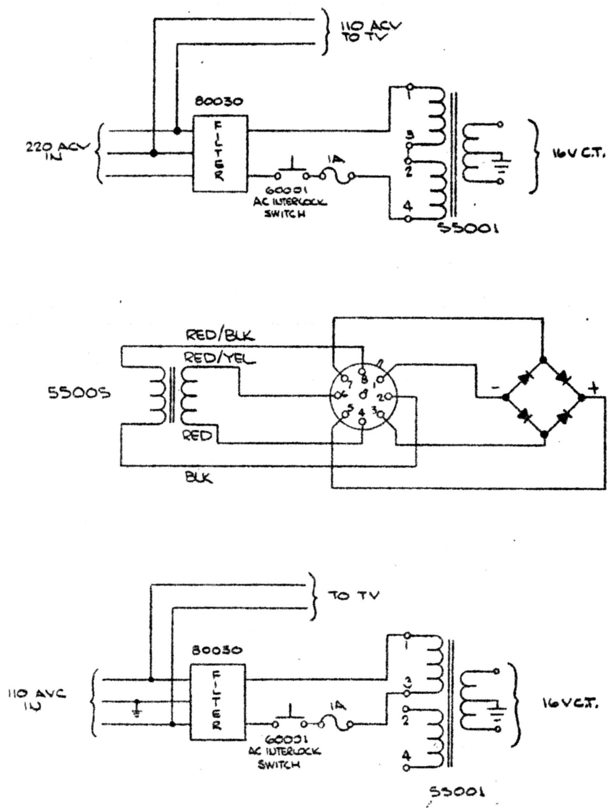
Schematic - Gotcha

Designer:

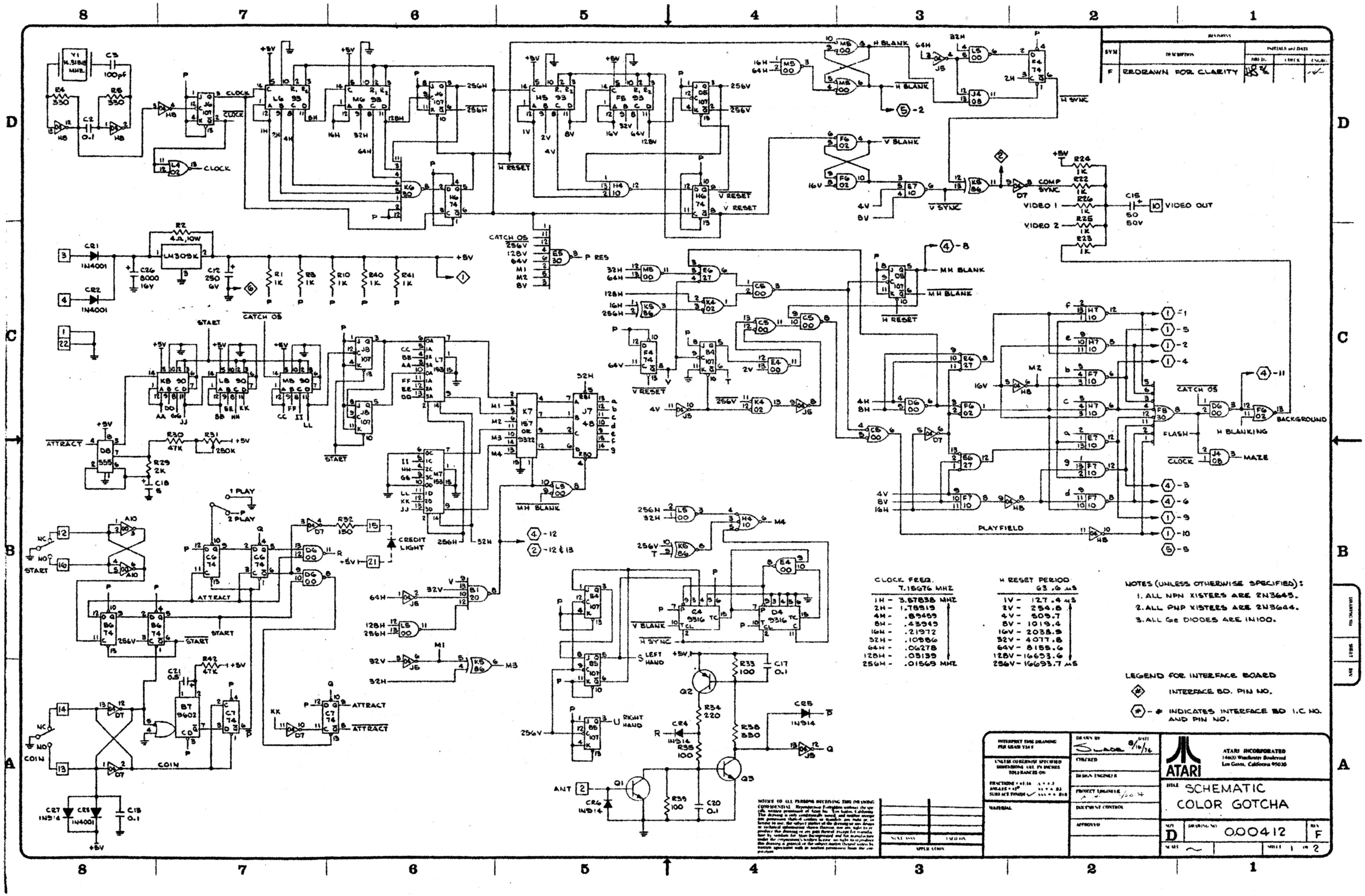
Drwn: PC Design App:
7-23-73 SH 2 of 2

REVISIONS

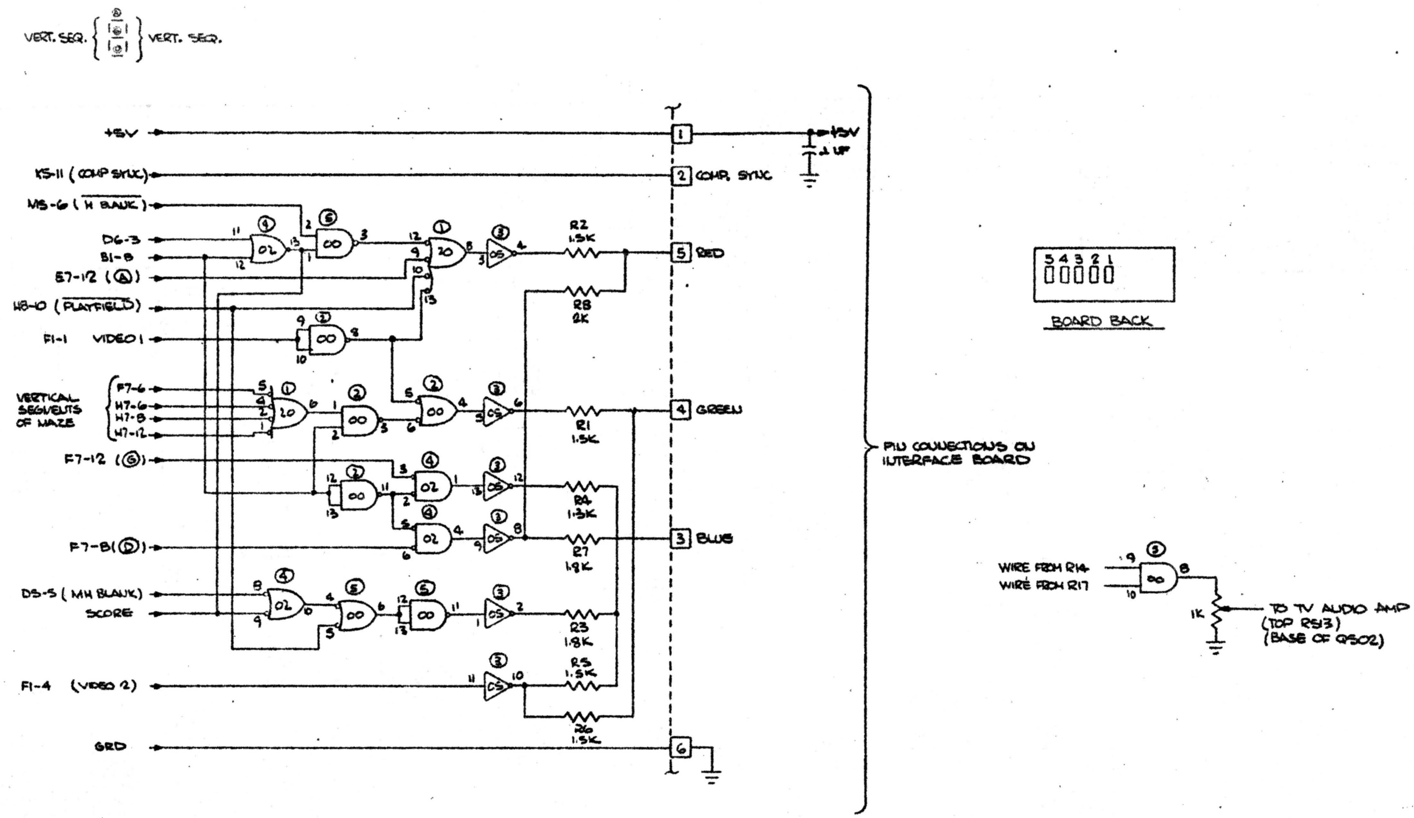
REV	DESCRIPTION	DATE	APPD
A	PROTOTYPE RELEASE	1-22-74	



ATARI, INC.	14600 WINCHESTER BLVD LOS GATOS, CAL	
SCALE: —	APPROVED BY:	DRAWN BY DC
DATE: 1-22-74		REVISED
SCHEMATIC DIAGRAM POWER SUPPLY		
COLOR GOTCHA		DRAWING NUMBER 000403



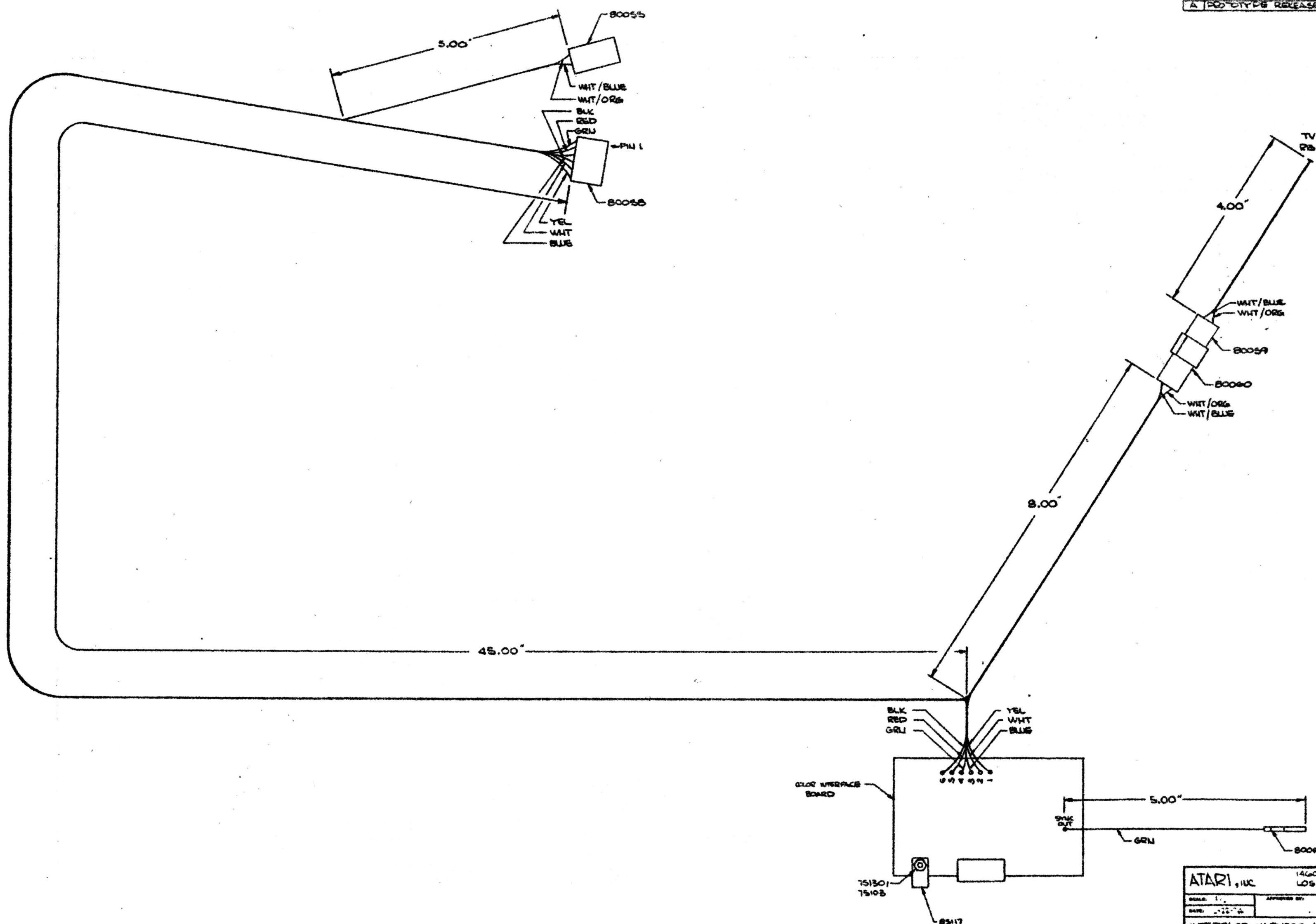
F REDRAWN FOR CLARITY
NOTES (UNLESS OTHERWISE SPECIFIED):
1. ALL NPN XISTERS ARE 2N3643.
2. ALL PNP XISTERS ARE 2N3644.
3. ALL Ge DIODES ARE IN100.
LEGEND FOR INTERFACE BOARD
INTERFACE BD. PIN NO.
- # INDICATES INTERFACE BD I.C NO. AND PIN NO.
CLOCK FREQ. 7.15676 MHZ
1H - 3.57838 MHZ
2H - 1.78919
4H - .89459
8H - .43945
16H - .21972
32H - .10986
64H - .06278
128H - .03139
256H - .01569 MHZ
H RESET PERIOD 63.6 μS
1V - 127.4 μS
2V - 254.8
4V - 509.7
8V - 1019.4
16V - 2038.9
32V - 4077.8
64V - 8155.6
128V - 16653.6
256V - 16693.7 μS
VIDEO OUT
PLAYFIELD
BACKGROUND
MAZE
CREDIT LIGHT
1 PLAY
2 PLAY
START
COIN
LEFT HAND
RIGHT HAND
ATARI
ATARI INCORPORATED
SCHEMATIC
COLOR GOTCHA
D
000412
F



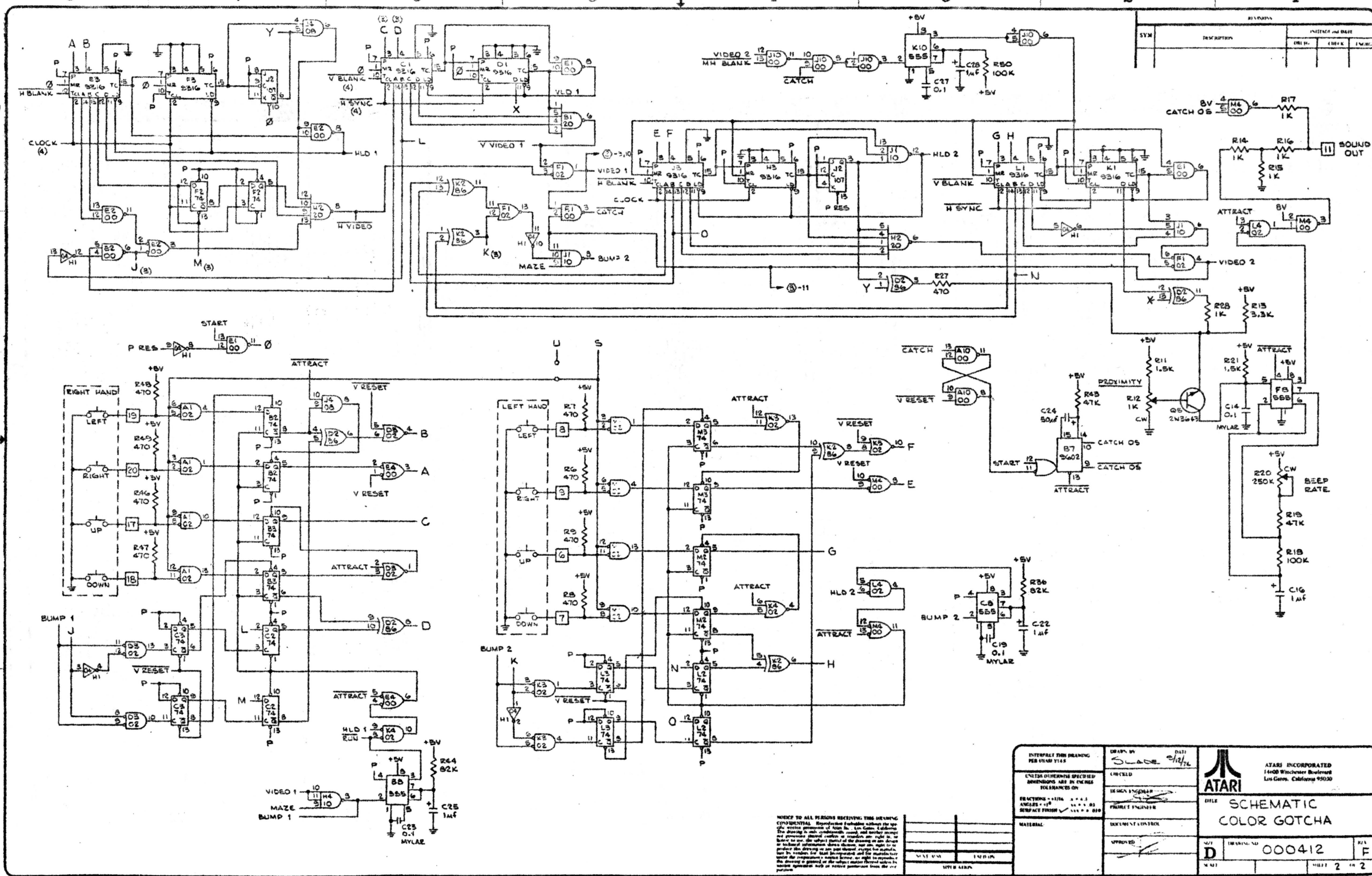
NOTES:
1. PIN NUMBERS SHOWN ARE FROM GOTCHA SCHEMATIC (REV F).

A	PROTOTYPE RELEASE	1-8-74
ATARI, INC	14600 WINCHESTER BLVD LOS GATOS, CAL	
SCALE: ———	APPROVED BY:	DRAWN BY DC
DATE: 1-4-73		REVISED
SCHEMATIC DIAGRAM GATING CIRCUIT FOR COLOR "GOTCHA"		
COLOR GOTCHA		DRAWING NUMBER .000402 A

REVISIONS			
REV	DESCRIPTION	DATE	APPD
A	PROTOTYPE RELEASE		



ATARI, INC	14600 WINCHESTER BLVD LOS GATOS, CAL
INTERFACE HARNESS ASSEMBLY	
COLOR GOTCHA	000411



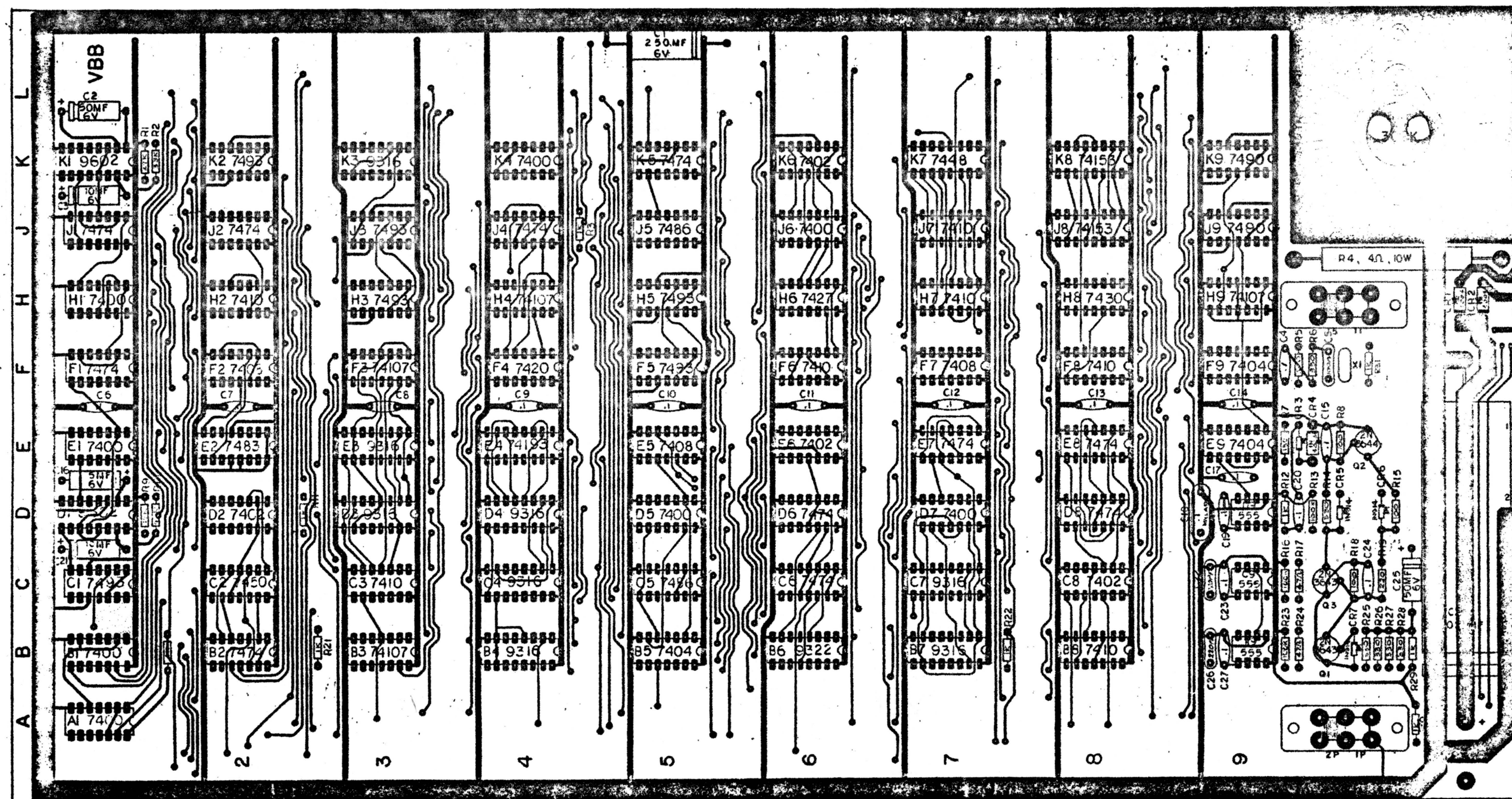
ATARI INCORPORATED
14600 Winchester Boulevard
Los Gatos, California 95030

SCHEMATIC
COLOR GOTCHA

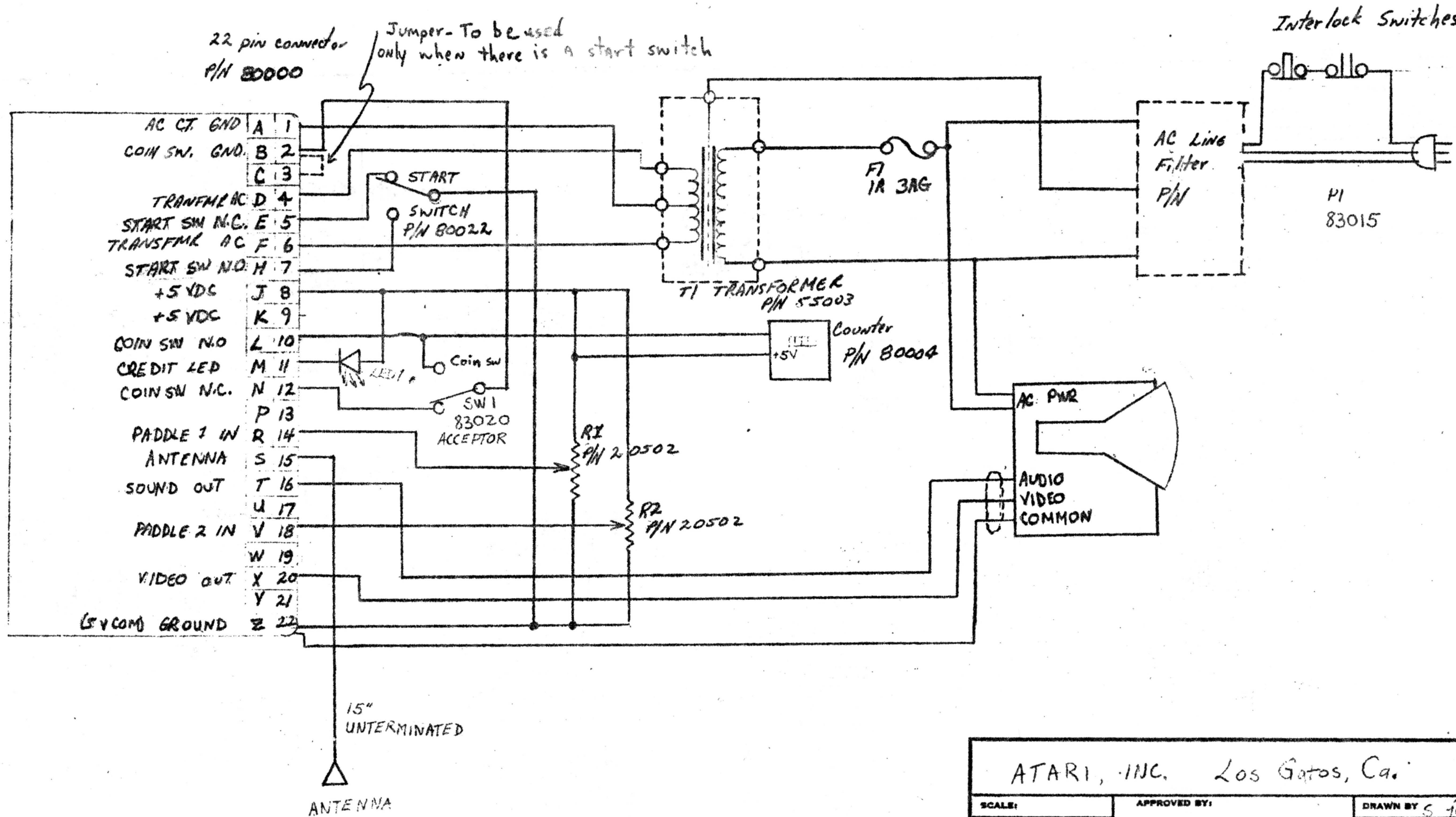
DRAWN BY SLADE 8/12/76

SIZE D DRAWING NO. 000412 REV F

SHEET 2 OF 2



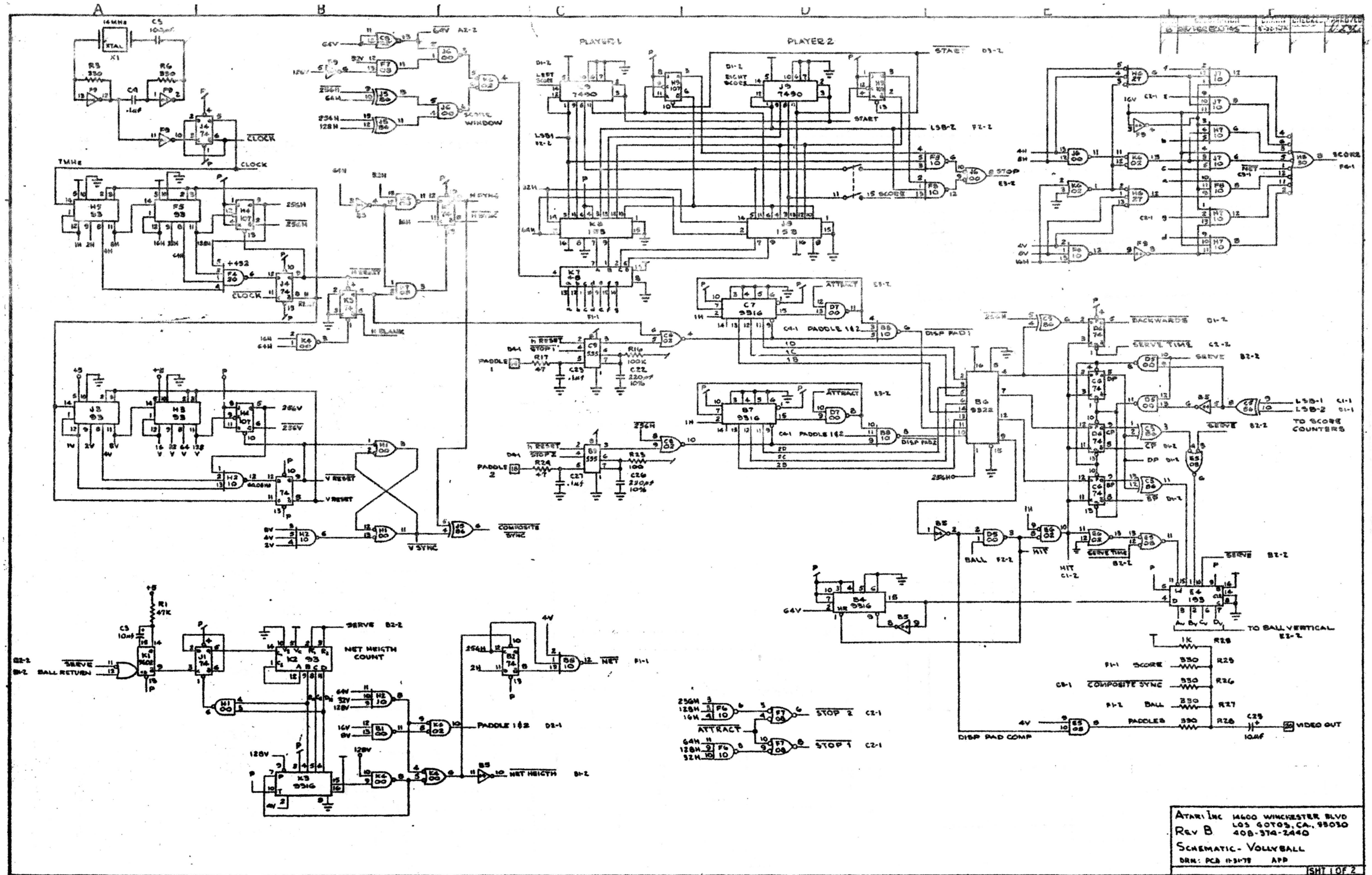
A000 846



* NOTE -
LED 1 IS CONTAINED
Within START SW, S2, 80022

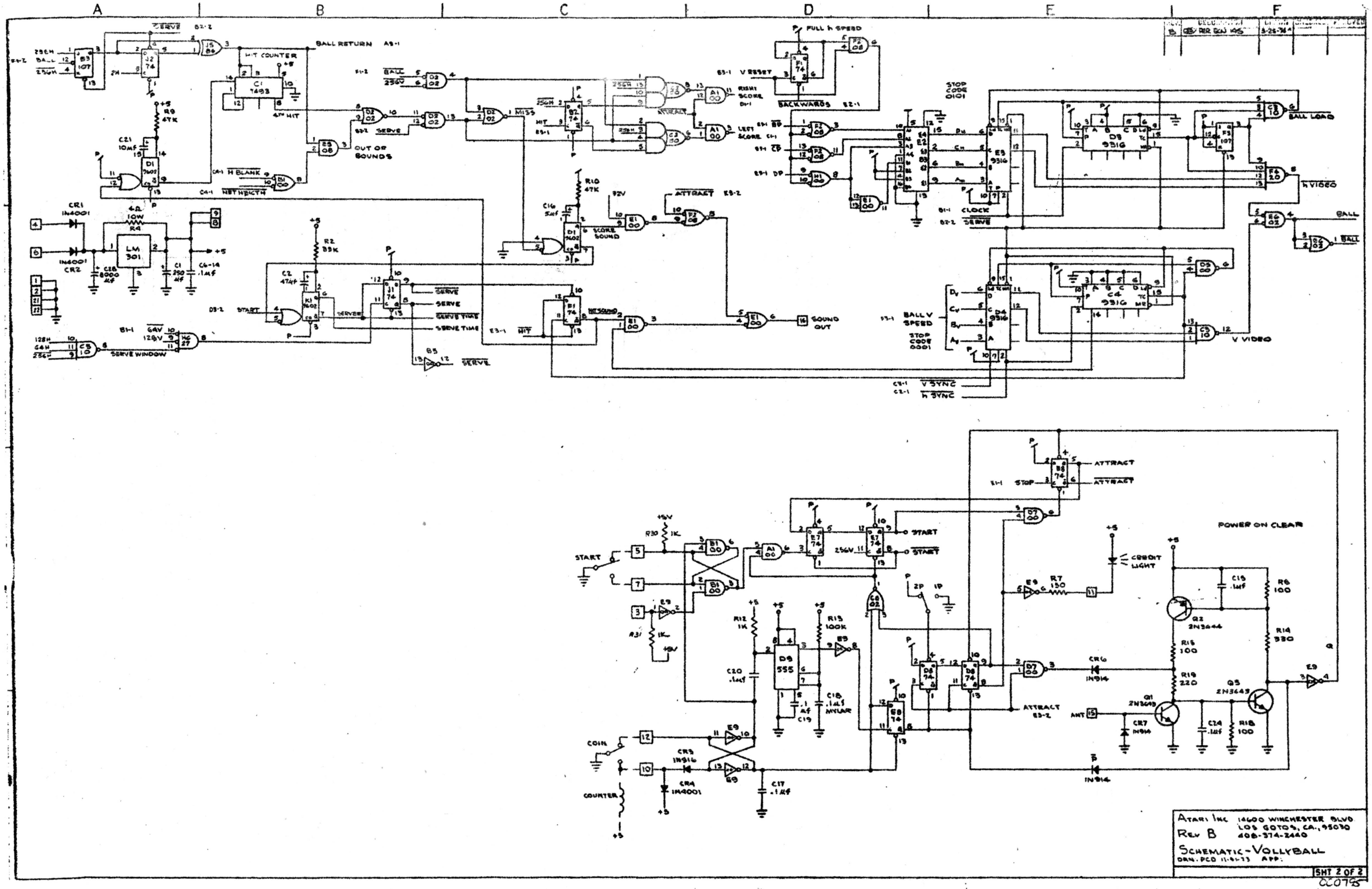
ATARI, INC. Los Gatos, Ca.		
SCALE:	APPROVED BY:	DRAWN BY S. Jobs
DATE: JAN 9, 1974		REVISED
ENCLOSURE WIRING, SCHEMATIC		
(VOLLEYBALL) REBOUND		DRAWING NUMBER 000515

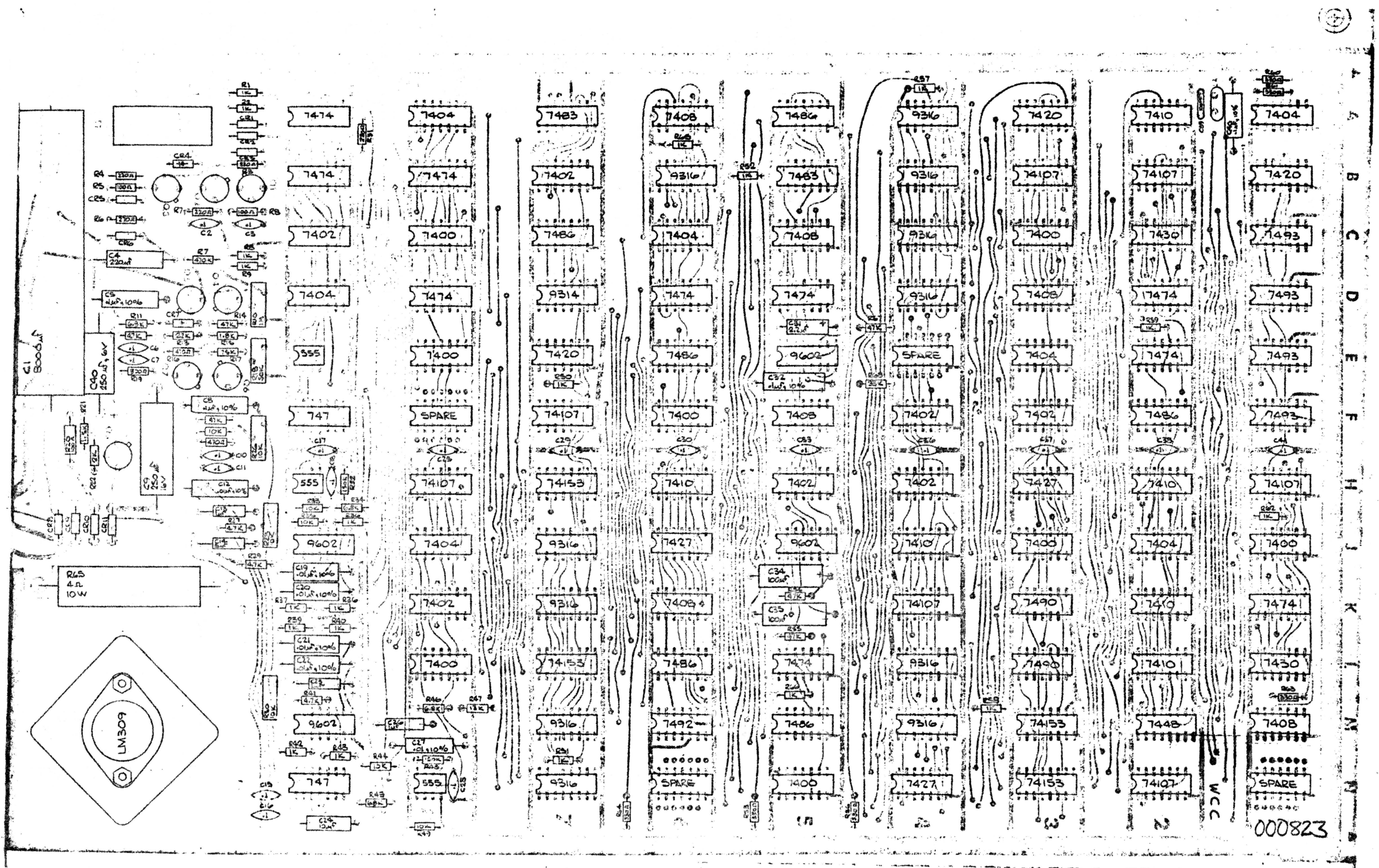
11X17 PRINTED ON NO. 1000H CLEARPRINT



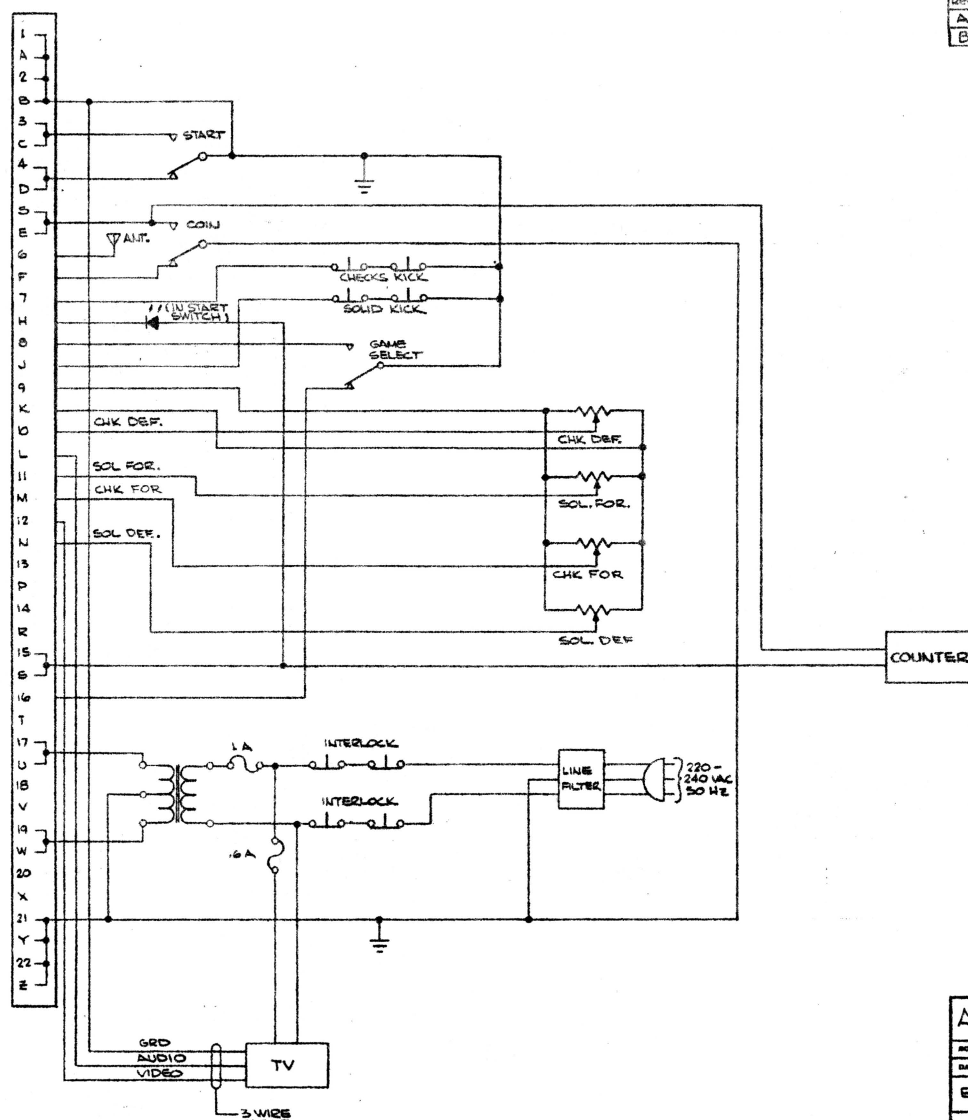
ATARI INC 14600 WINCHESTER BLVD
LOS GATOS, CA. 95030
408-374-2440
REV B
SCHEMATIC - VOLLYBALL
DRN: PCB 11-31-73 APP
SHT 1 OF 2
PLAYER 1
PLAYER 2
VIDEO OUT
TO SCORE COUNTERS
TO BALL VERTICAL
NET HEIGTH COUNT

008 795


Atari Inc
14600 Winchester Blvd
Los Gatos, Ca. 95030
408-374-2440
Rev B
Schematic-Vollyball
DRN. PCD 11-14-73 APP.
SHT 2 OF 2
CC075
POWER ON CLEAR
HIT COUNTER
BALL RETURN
OUT OF BOUNDS
SCORE SOUND
SOUND OUT
SERVE WINDOW
BALL V SPEED
STOP CODE 0001
STOP CODE 0101
BACKWARDS
FULL h SPEED
BALL LOAD
h VIDEO
V VIDEO
CREDIT LIGHT
START
COIN
COUNTER
ATTRACT


LM309
R45 4Ω 10W
C1 8000uF
C40 250uF, 6V
WCC
000823
A B C D E F H J K L M N

REVISION			
REV	DESCRIPTION	DATE	APPD
A	PRODUCTION RELEASE	2-12-74	
B	CHANGED PER ECN # 84	3-5-74	CG



ATARI, INC 14600 WINCHESTER BLVD LOS GATOS, CAL

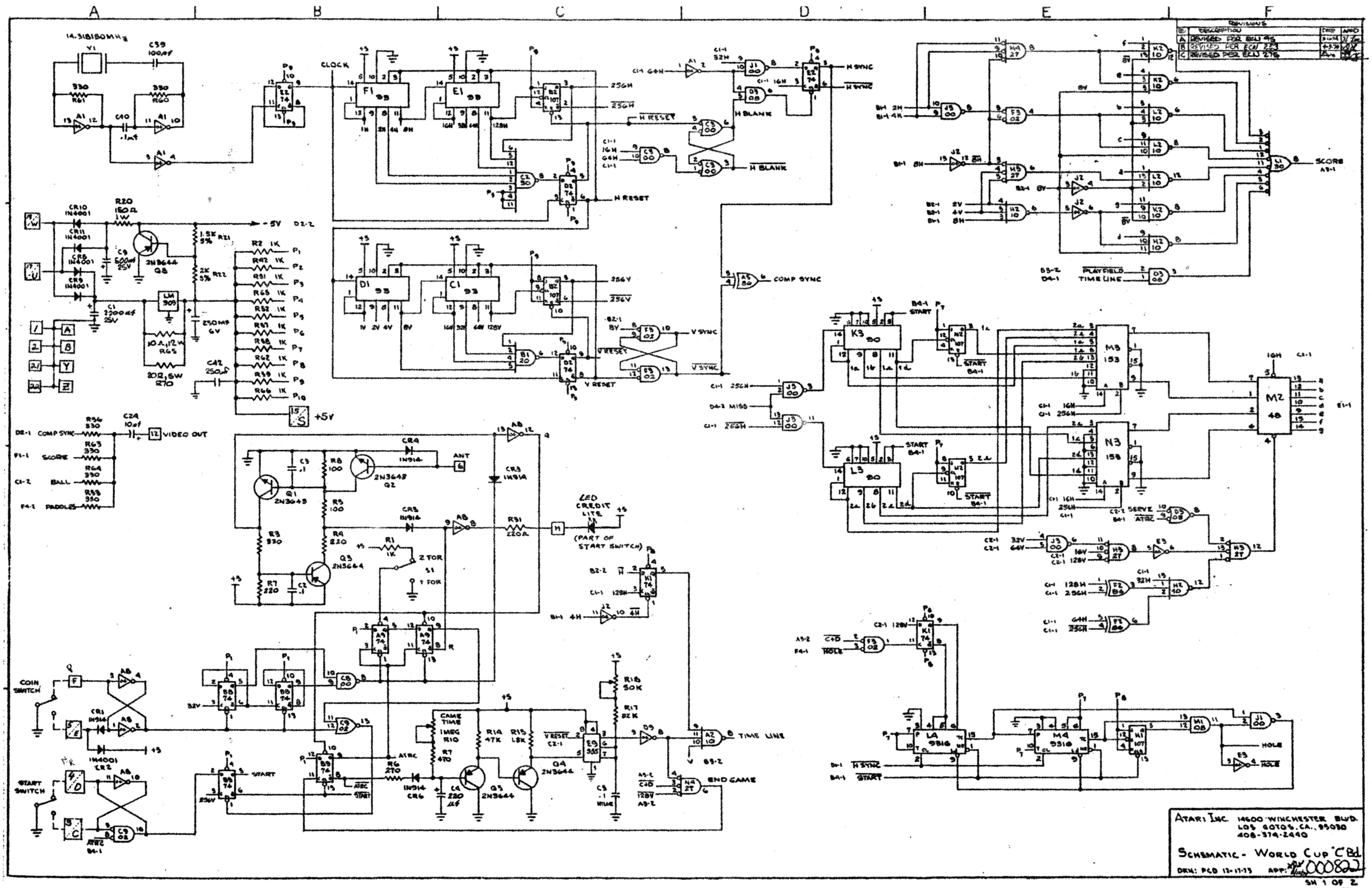
SCALE: — APPROVED BY: Larry Leppert 2/12/74 DRAWN BY DC

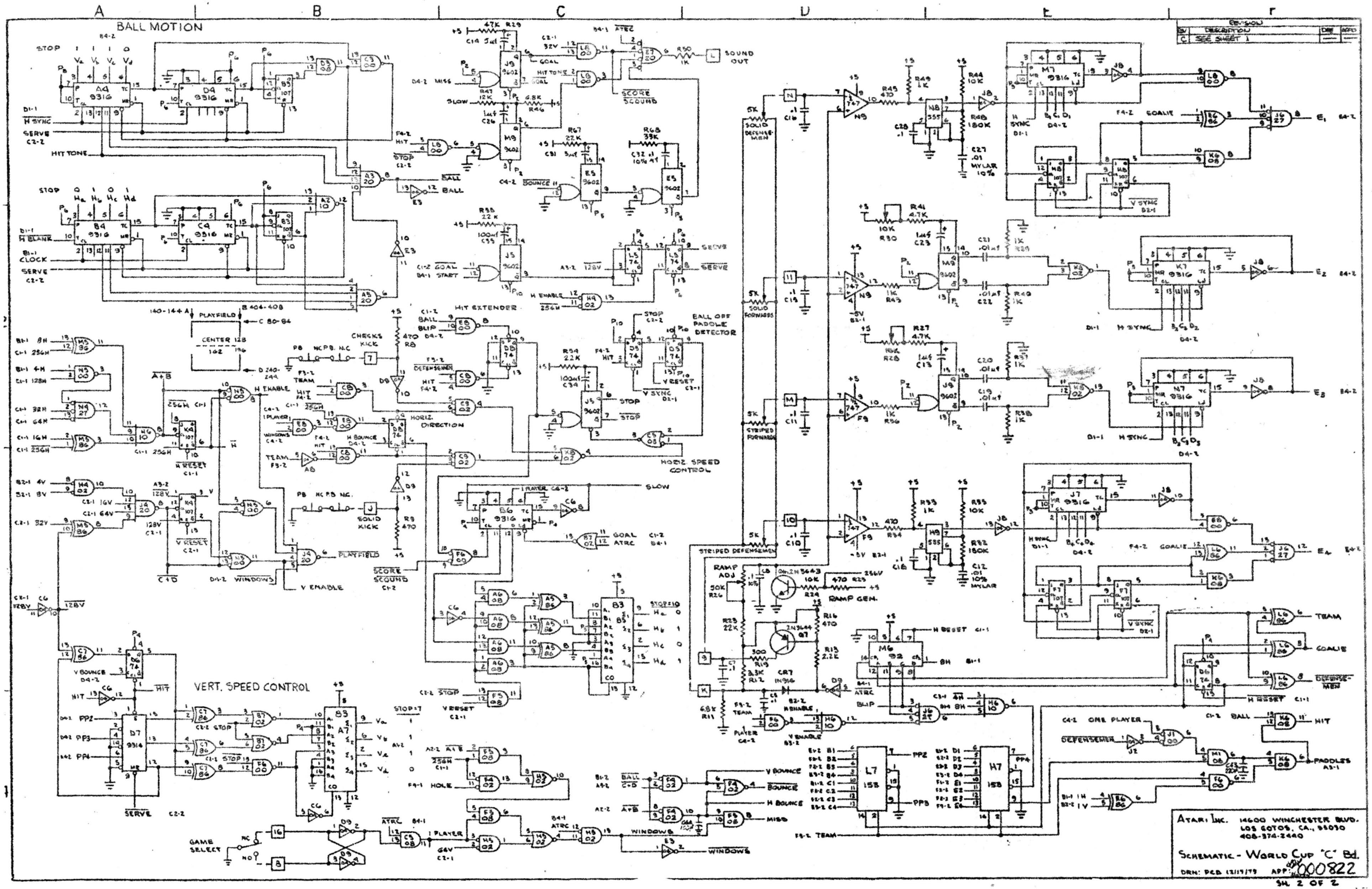
DATE: 2-12-74 REVISED

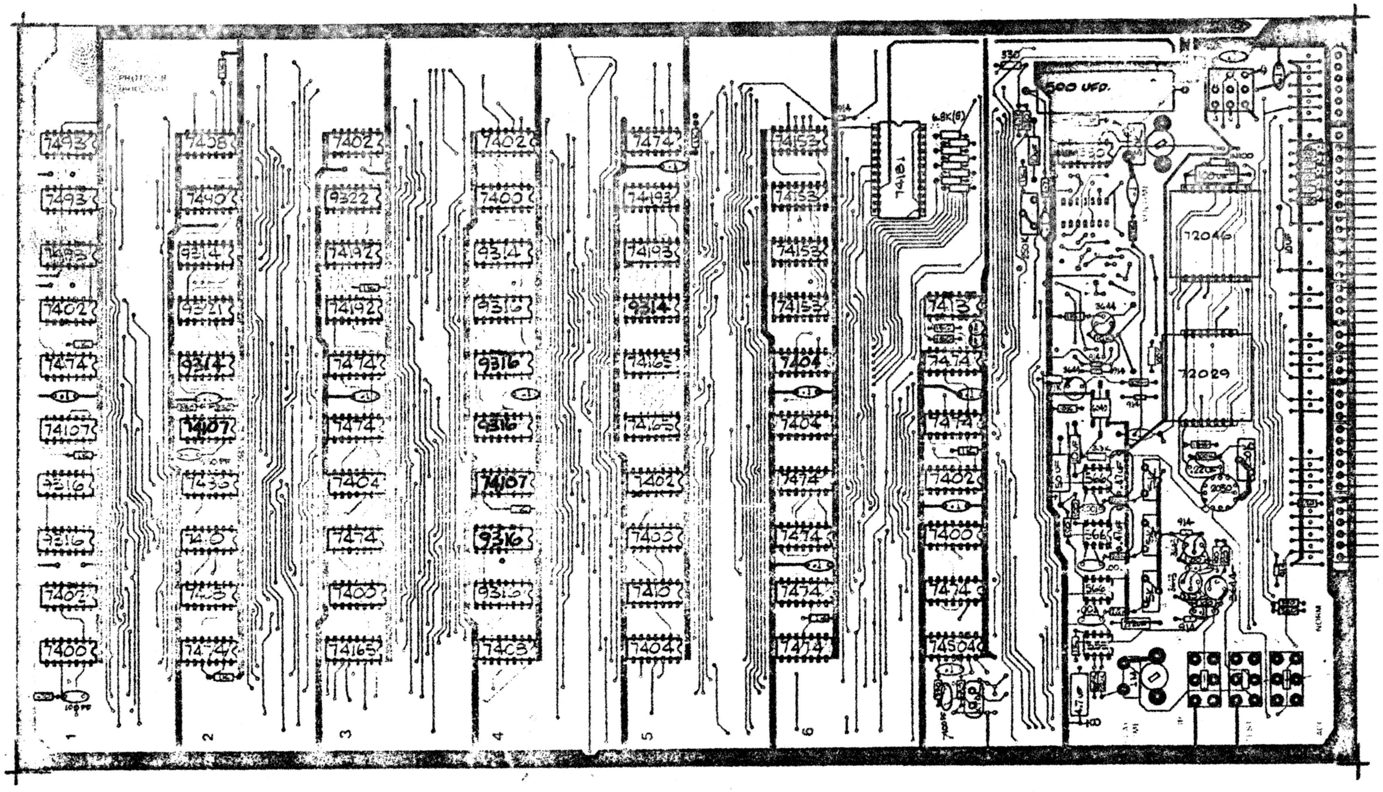
ENCLOSURE, WIRING DIAGRAM

WORLD CUP

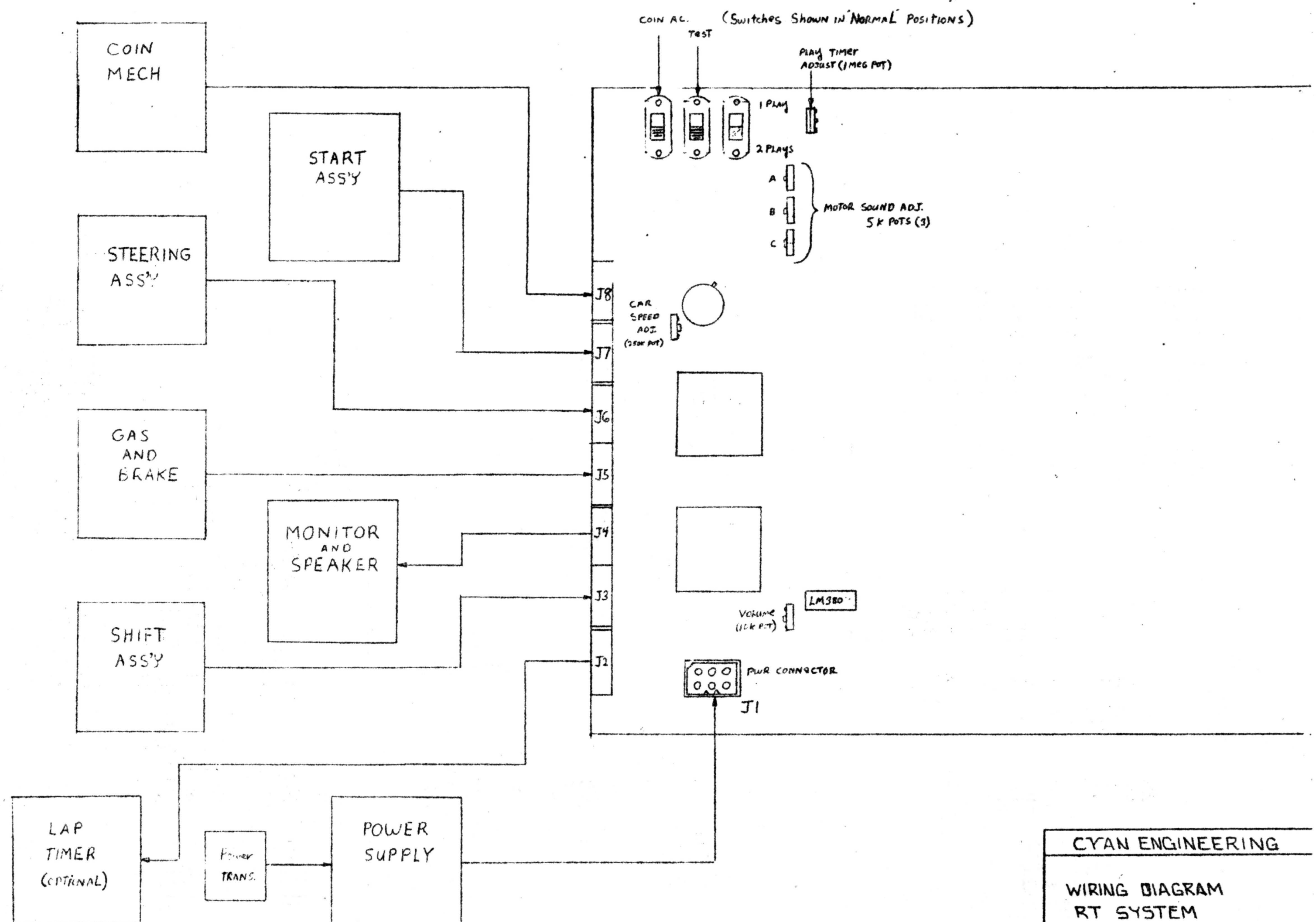
DRAWING NUMBER 000906


REVISIONS
DESCRIPTION
A REVISED PER ECN 95
B REVISED PER ECN 223
C REVISED PER ECN 276
CLOCK
H SYNC
COMP SYNC
V SYNC
H BLANK
H RESET
V RESET
SCORE
PLAYFIELD
TIME LINE
VIDEO OUT
COMP SYNC
SCORE
BALL
PADDLES
COIN SWITCH
START SWITCH
LED CREDIT LITE
(PART OF START SWITCH)
GAME TIME
END GAME
SERVE
HOLE
START
ANT
+5V
-5V
14.31818 MHz
Atari Inc. 14600 Winchester Blvd. Los Gatos, CA. 95030 408-374-2440
Schematic - World Cup 'C' Bd.
DRN: PCD 12-17-73
SH 1 OF 2


BALL MOTION
VERT. SPEED CONTROL
HORIZ. SPEED CONTROL
HIT EXTENDER
BALL OFF PADDLE DETECTOR
RAMP GEN.
SOUND OUT
REVISION
SEE SHEET 1
ATARI INC. 14600 WINCHESTER BLVD. LOS GATOS, CA., 95030 408-374-2440
SCHEMATIC - WORLD CUP "C" Bd.
DRN: PCB 12/19/79
000822
SH. 2 OF 2



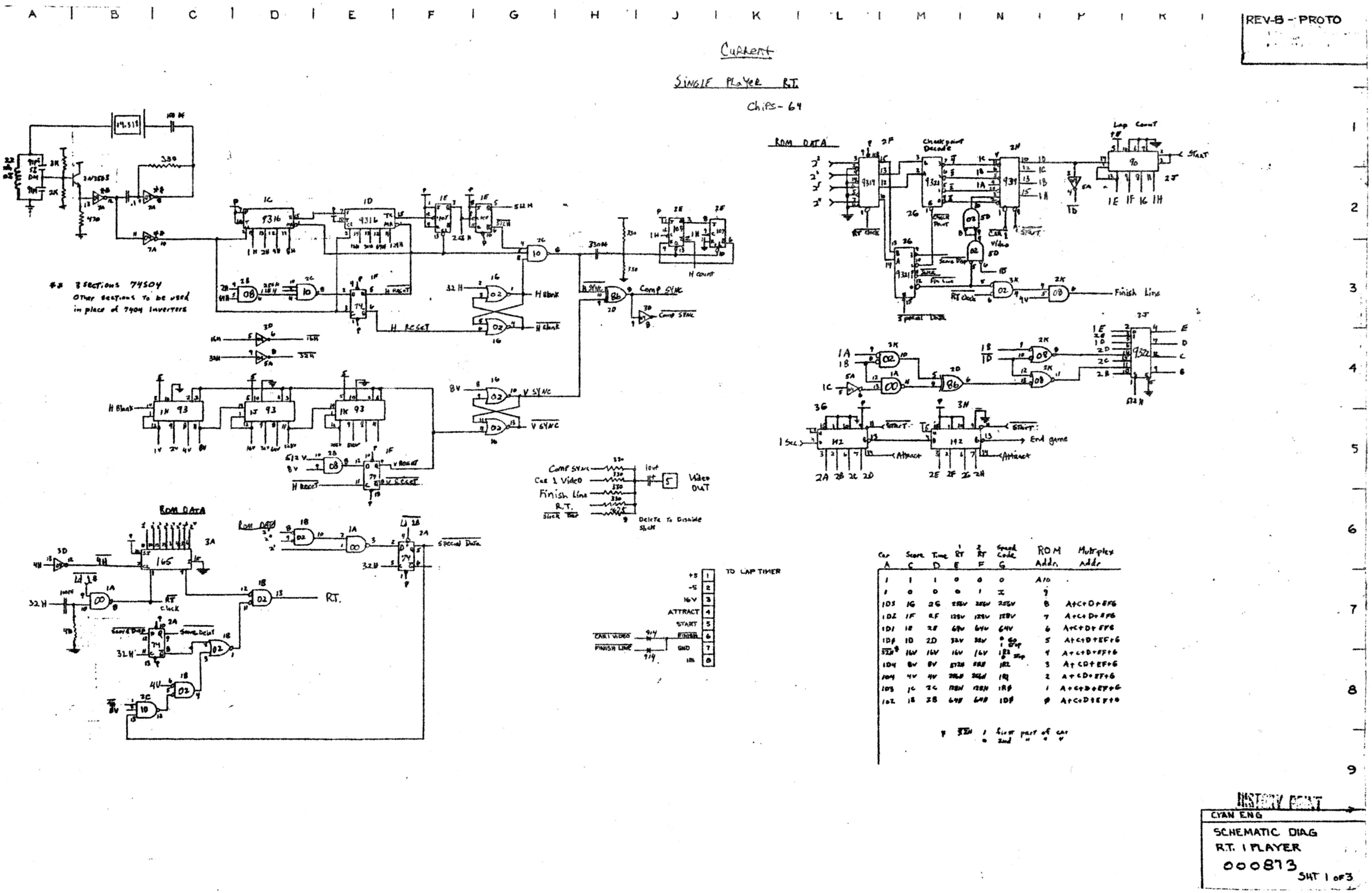
GRAN TRAK 10
REV. 'B'
DWG. NO. 000872

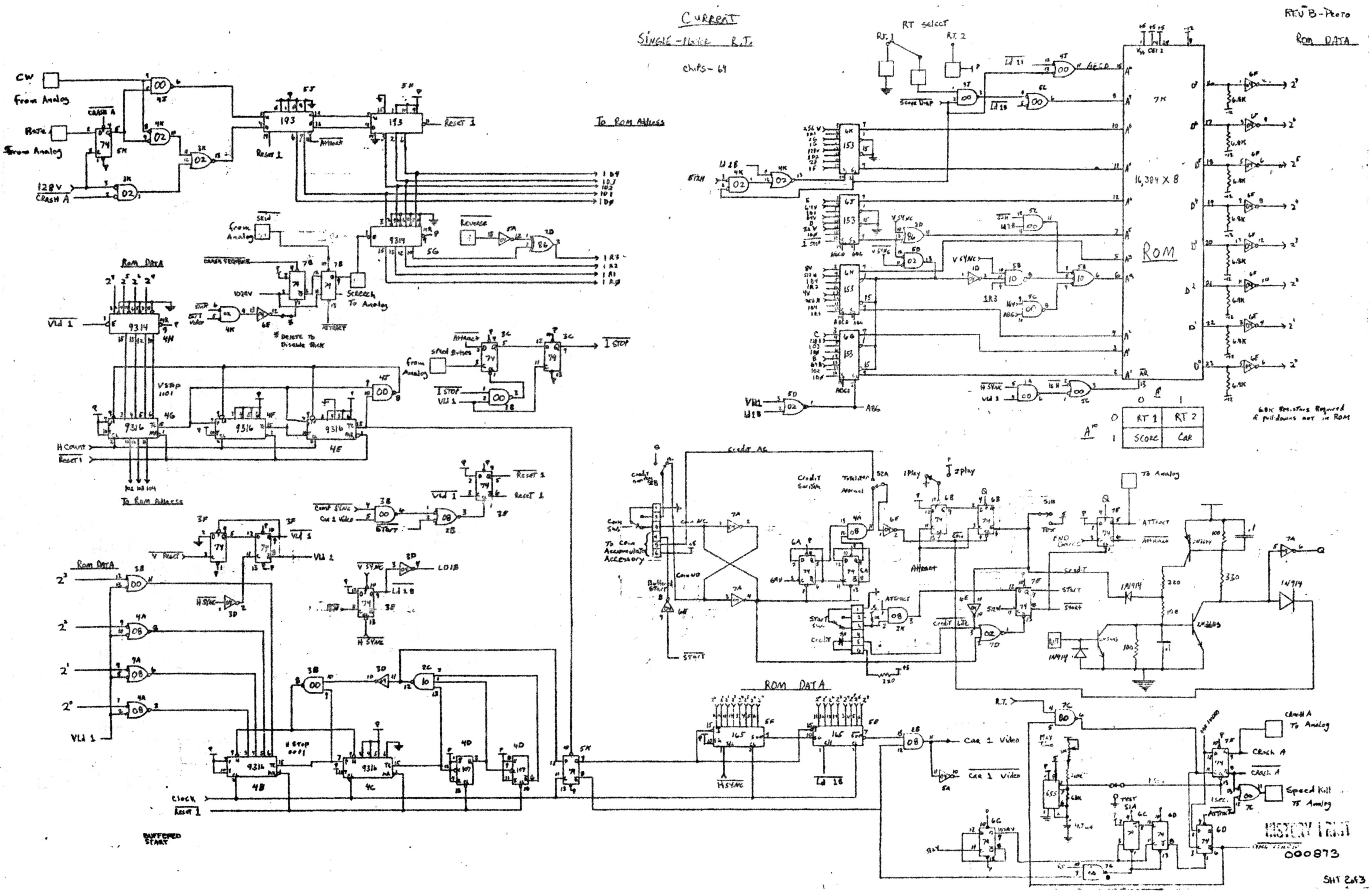


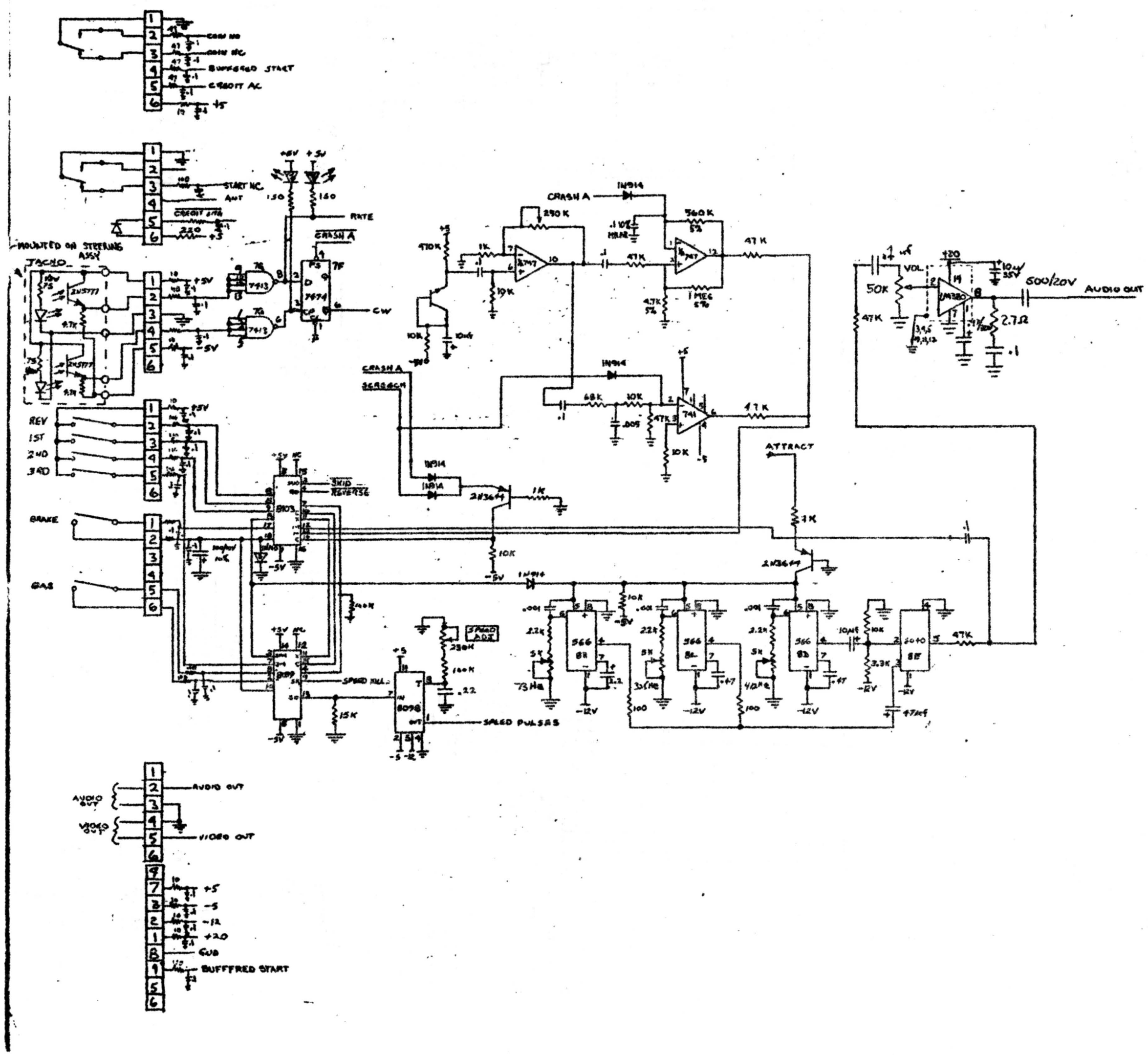
CYAN ENGINEERING

WIRING DIAGRAM
RT SYSTEM
Dd. 3/20/78

000858


REV-B - PROTO
Current
Single Player R.T.
Chips - 64
ROM DATA
Checkpoint Decode
Lap Count
START
Finish Line
Comp SYNC
H Blank
H RESET
V SYNC
V RESET
H count
End game
Attract
Video OUT
Delete to Disable Skid
TO LAP TIMER
+5
-5
16V
ATTRACT
START
FINISH
GND
CAR 1 VIDEO
FINISH LINE
Special Data
R.T.
ROM Addr.
Multiplex Addr
CYAN ENG
SCHEMATIC DIAG
R.T. 1 PLAYER
000873
SHT 1 of 3

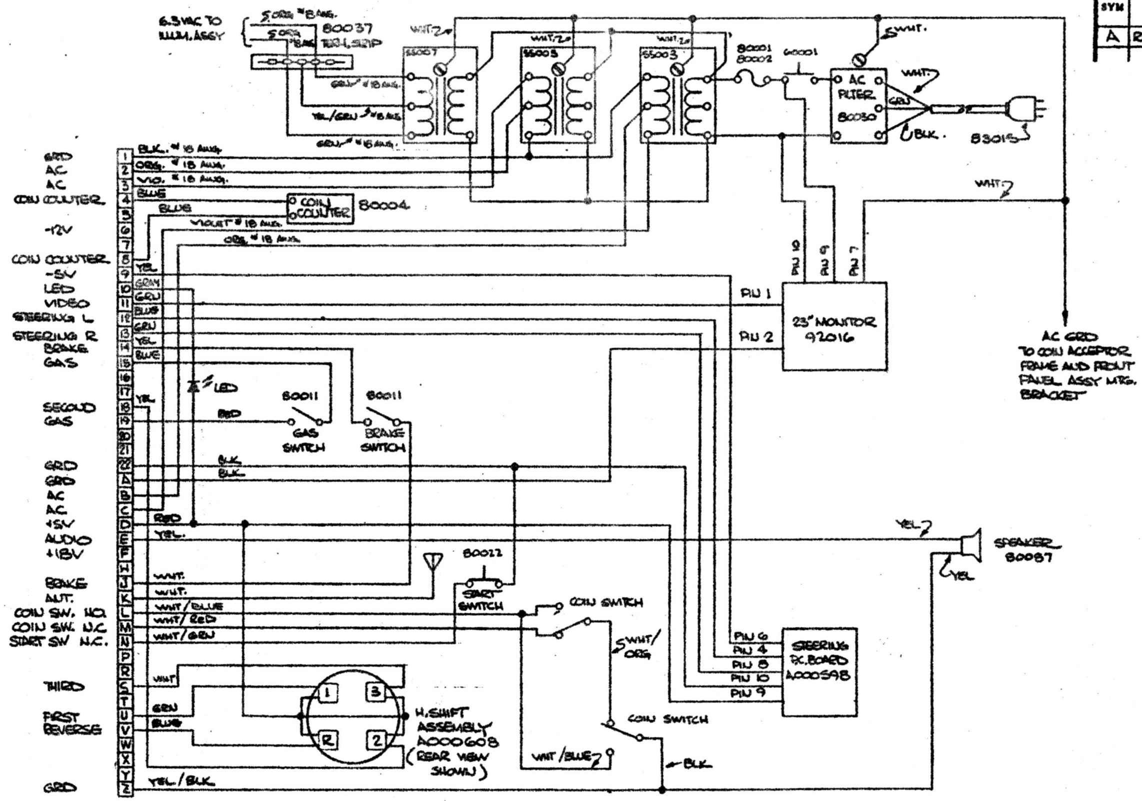

Current
Single-Player R.T.
Chips - 64
REV B-Proto
Rom Data
To Rom Address
16,384 X 8
ROM
68K Resistors Required if pulldowns not in ROM
RT 1
RT 2
Score
Car
RT select
ROM DATA
Car 1 Video
Speed Kill To Analog
Crash A To Analog
To Analog
000873
SHT 2 of 3



11/29/73 HISTORY FILE
12/12/73

000873
SHT 3 of 3

SYM	DESCRIPTION	DRFTG	CHECK	ENGRG
A	RELEASED FOR PRODUCTION	3-18-74		4/3/74



NOTES:
1. ALL WIRE TO BE #20AWG UNLESS OTHERWISE SPECIFIED.

000519	GT-10
NEXT ASSY	USED ON
APPLICATION	

INTERPRET THIS DRAWING PER USASI Y14.5

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON:
FRACTIONS = ±1/16 .x = ±.1
ANGLES = ±1° .xx = ±.03
SURFACE FINISH ✓ .xxx = ±.010

MATERIAL:

DRAWN BY DC DATE 3-18-74
CHECKED
DESIGN ENGINEER
PROJECT ENGINEER JERRY DONALDSON 4/3/74
DOCUMENT CONTROL
APPROVED

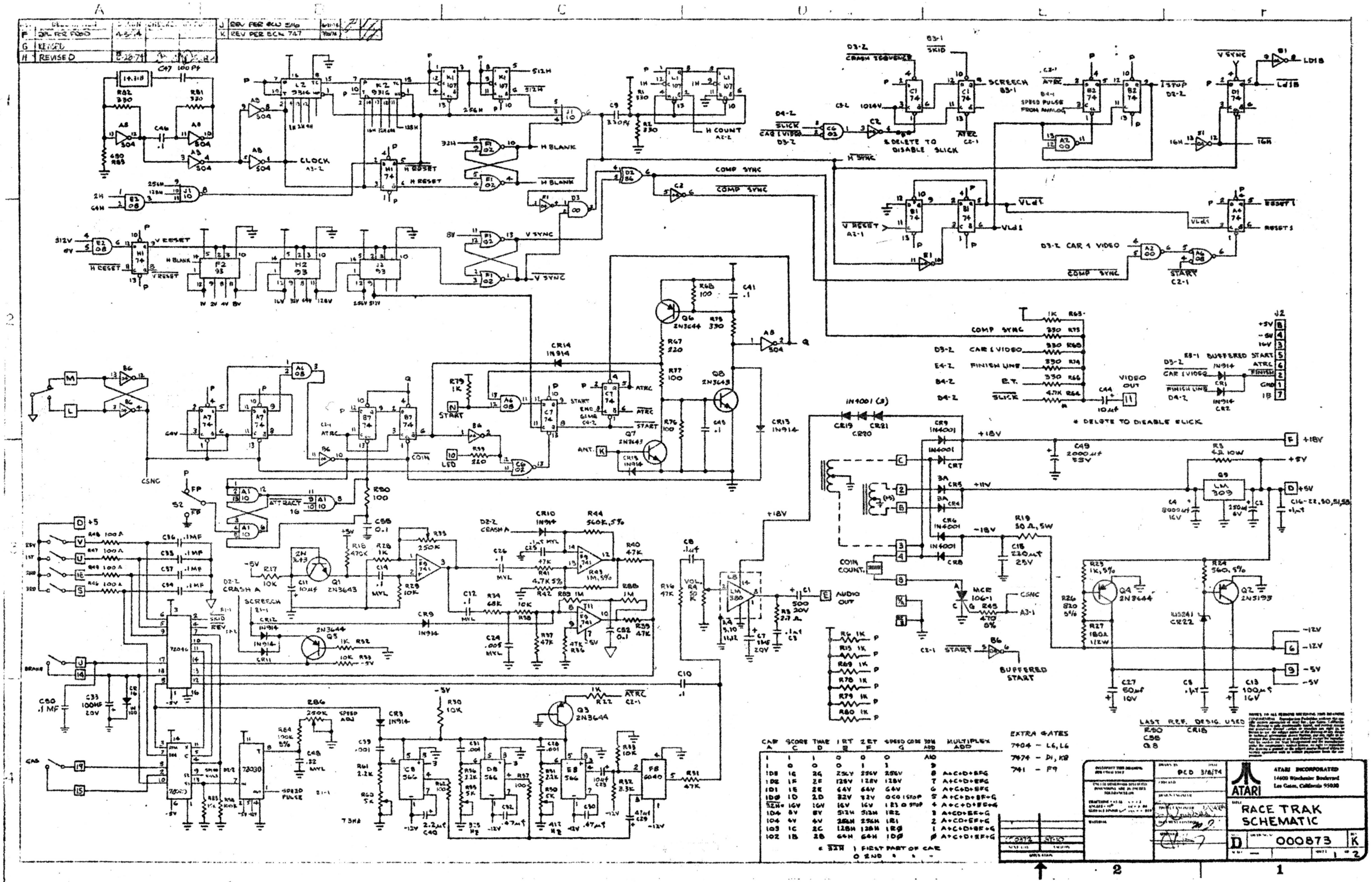
ATARI

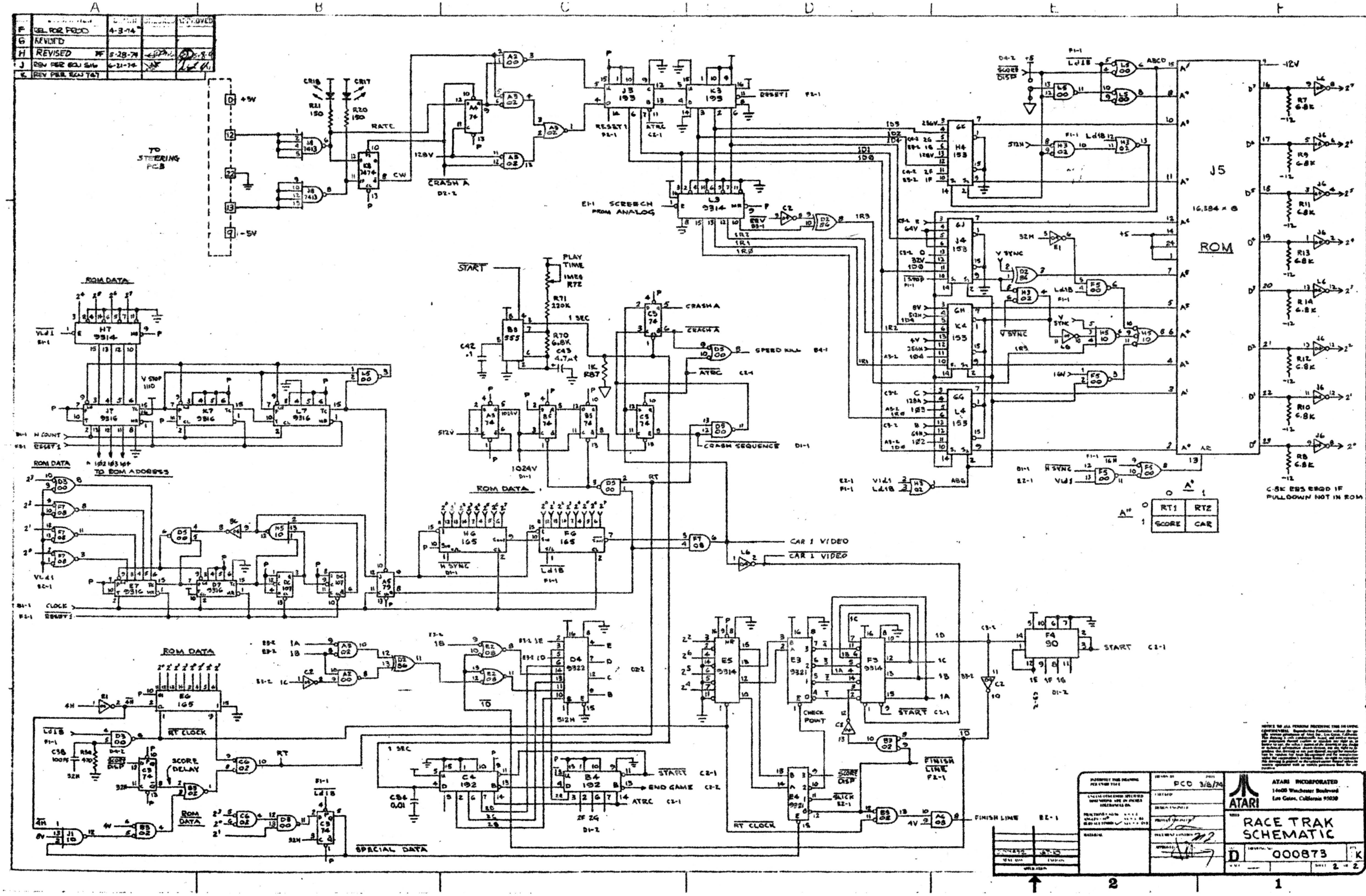
ATARI INCORPORATED
14600 Winchester Boulevard
Los Gatos, California 95030

TITLE WIRING ENCLOSURE DIAGRAM
GRAN TRAK 10

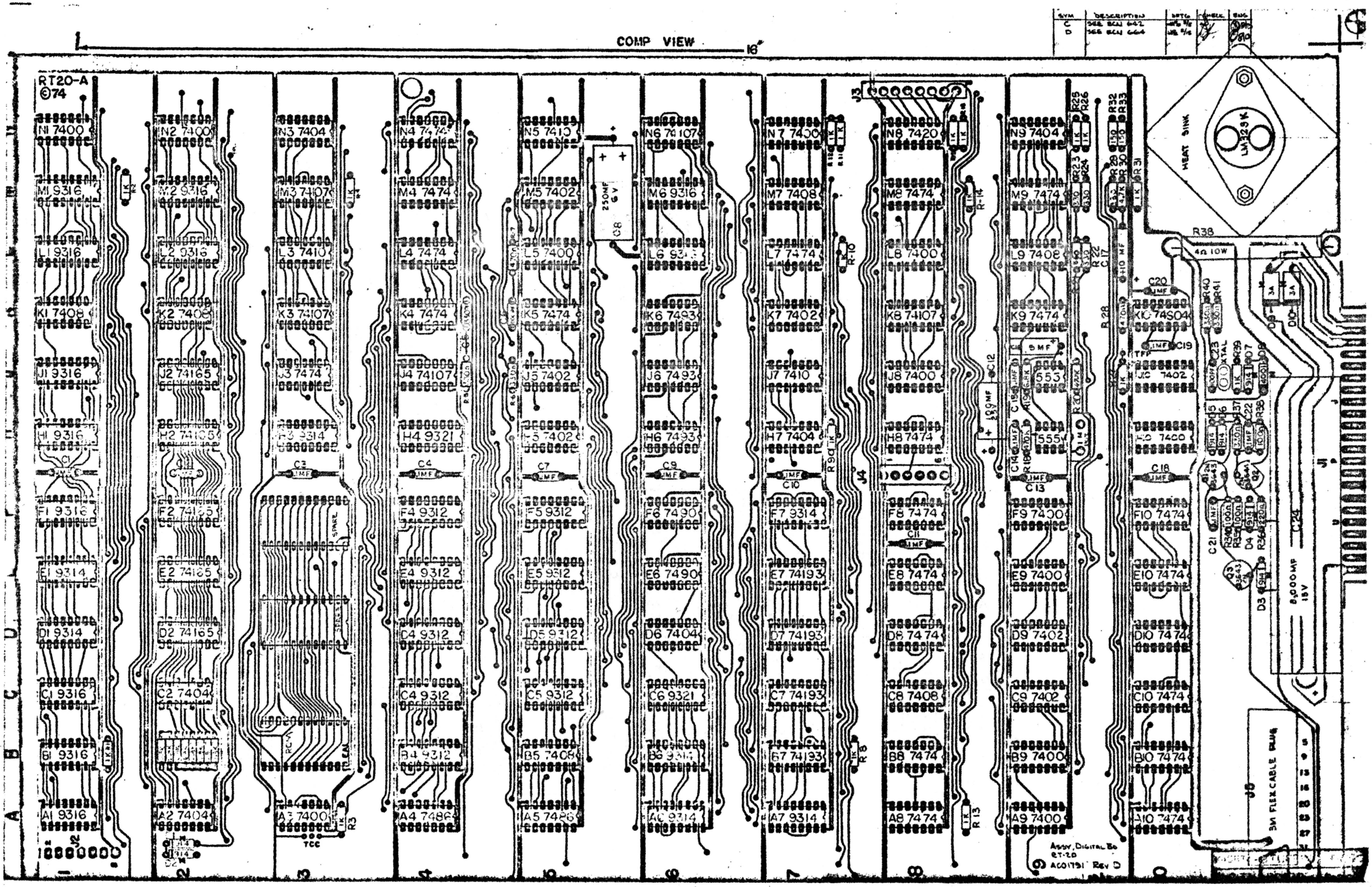
SIZE C DRAWING NO. 001060 REV A
SCALE — SHEET 1 OF 1

DRAWING NO. 001060 SHEET 1 REV A


RACE TRAK
SCHEMATIC
ATARI INCORPORATED
14600 Winchester Boulevard
Los Gatos, California 95030
D
000873
K
1 of 2
DCD 3/8/74
REV PER ECN 516
REV PER ECN 747
REVISED
EXTRA GATES
7404 - L6, L6
7474 - D1, K8
741 - F9
LAST REF. DESIG. USED
R80 CR18
C58
Q8
CLOCK
H BLANK
H RESET
V RESET
V SYNC
COMP SYNC
H COUNT
SCREECH
SPEED PULSE FROM ANALOG
& DELETE TO DISABLE SLICK
* DELETE TO DISABLE SLICK
VIDEO OUT
AUDIO OUT
COIN COUNT.
BUFFERED START
CRASH A
ATTRACT
LED
START
SPEED PULSE
SPEED ADJ
BRAKE
GAS
CSNC

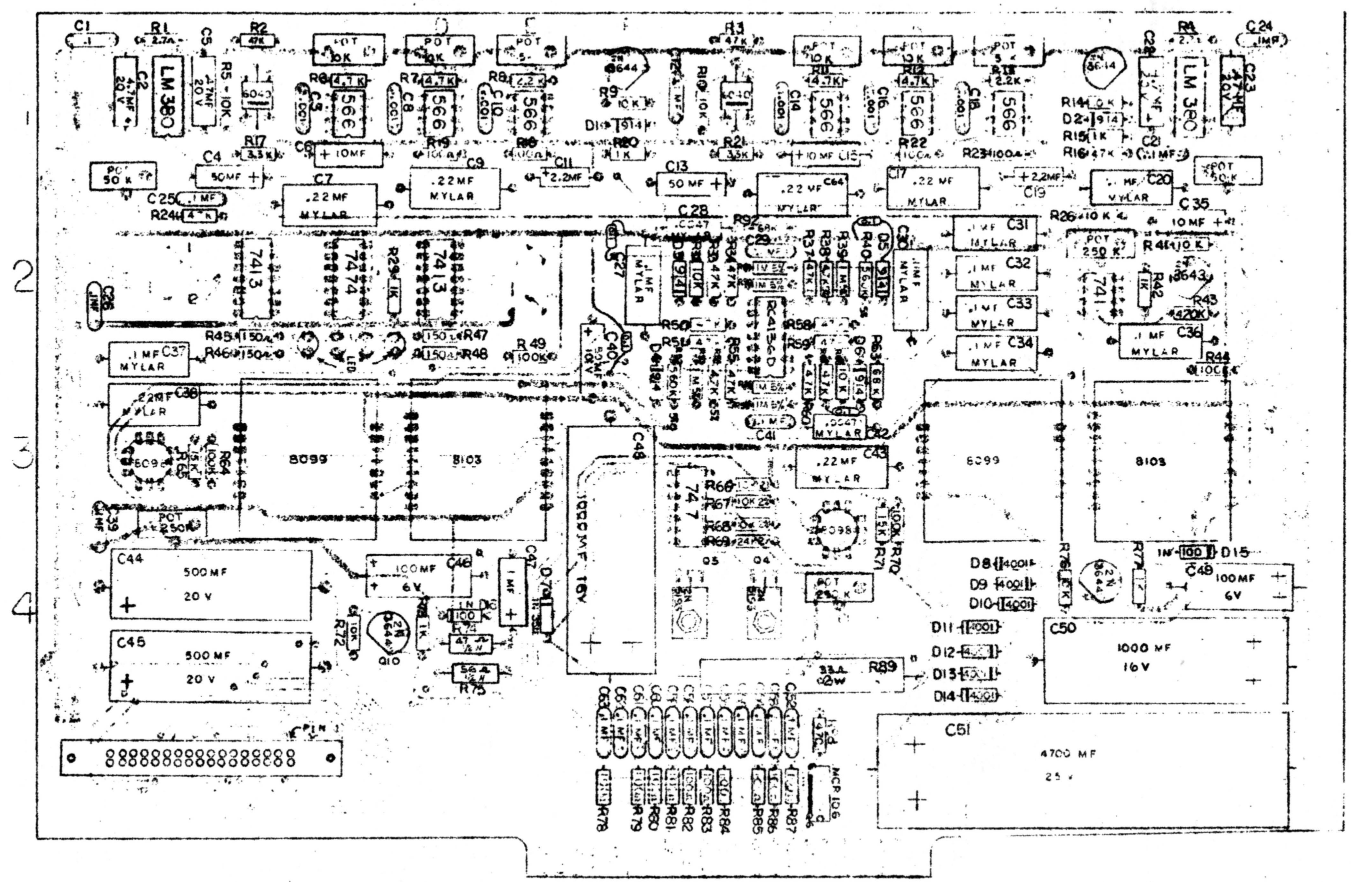


RACE TRAK SCHEMATIC
ATARI INCORPORATED
D 000873
REL FOR PROD 4-3-74
REVISED
REVISED 5-28-74
REV PER ECU 6-21-74
TO STEERING PCB
ROM
J5
16,384 × 8
ROM DATA
TO ROM ADDRESS
CAR 1 VIDEO
CRASH SEQUENCE
SPEED KILL
SCREECH FROM ANALOG
PLAY TIME
START
END GAME
FINISH LINE
RT CLOCK
SCORE DELAY
SPECIAL DATA
CHECK POINT
6.8K EBS E8QD IF PULLDOWN NOT IN ROM
RT1
RT2
SCORE
CAR



SYM DESCRIPTION
C SEE ECN 642
D SEE ECN 664
COMP VIEW
16"
RT20-A
©74
HEAT SINK
LM323K
R38
4Ω 10W
N1 7400
M1 9316
L1 9316
K1 7408
J1 9316
H1 9316
F1 9316
E1 9314
D1 9314
C1 9316
B1 9316
A1 9316
N2 7400
M2 9316
L2 9316
K2 7408
J2 74165
H2 74165
F2 74165
E2 74165
D2 74165
C2 7404
A2 7404
N3 7404
M3 74107
L3 74107
K3 74107
J3 7474
H3 9314
A3 7400
N4 7474
M4 7474
L4 7474
K4 7474
J4 74107
H4 9321
F4 9312
E4 9312
D4 9312
C4 9312
B4 9312
A4 7486
N5 7410
M5 7402
L5 7400
K5 7474
J5 7402
H5 7402
F5 9312
E5 9312
D5 9312
C5 9312
B5 7408
A5 7486
250MF 6V
C8
N6 74107
M6 9316
K6 7493
J6 7493
H6 7493
F6 7490
E6 7490
D6 7404
C6 9321
N7 7400
M7 7408
L7 7474
K7 7402
J7 7410
H7 7404
F7 9314
E7 74193
D7 74193
C7 74193
B7 74193
A7 9314
J3
J4
N8 7420
M8 7474
L8 7400
K8 74107
J8 7400
H8 7474
F8 7474
E8 7474
D8 7474
C8 7408
B8 7474
A8 7474
N9 7404
M9 7474
L9 7408
K9 7474
555
555
F9 7400
E9 7400
D9 7402
C9 7402
B9 7400
A9 7400
K10 74S04
F10 7474
E10 7474
D10 7474
C10 7474
B10 7474
A10 7474
8,000MF 15V
3M FLEX CABLE PLUG
J1
J6
Assy, Digital Bd
RT-20
AC01791 Rev D

SYM	DESCRIPTION	DFTG	CHECK	ENG
C	SEE ECN 643	[illegible]		8/13
D	REV PER ECN 663	8-15-74		8/20
E	REV PER ECN 658 683	8-5-74		8/20
F	REV PER ECN 704	9-5-74		
G	REV PER ECN 794	9-27-74		



ATARI

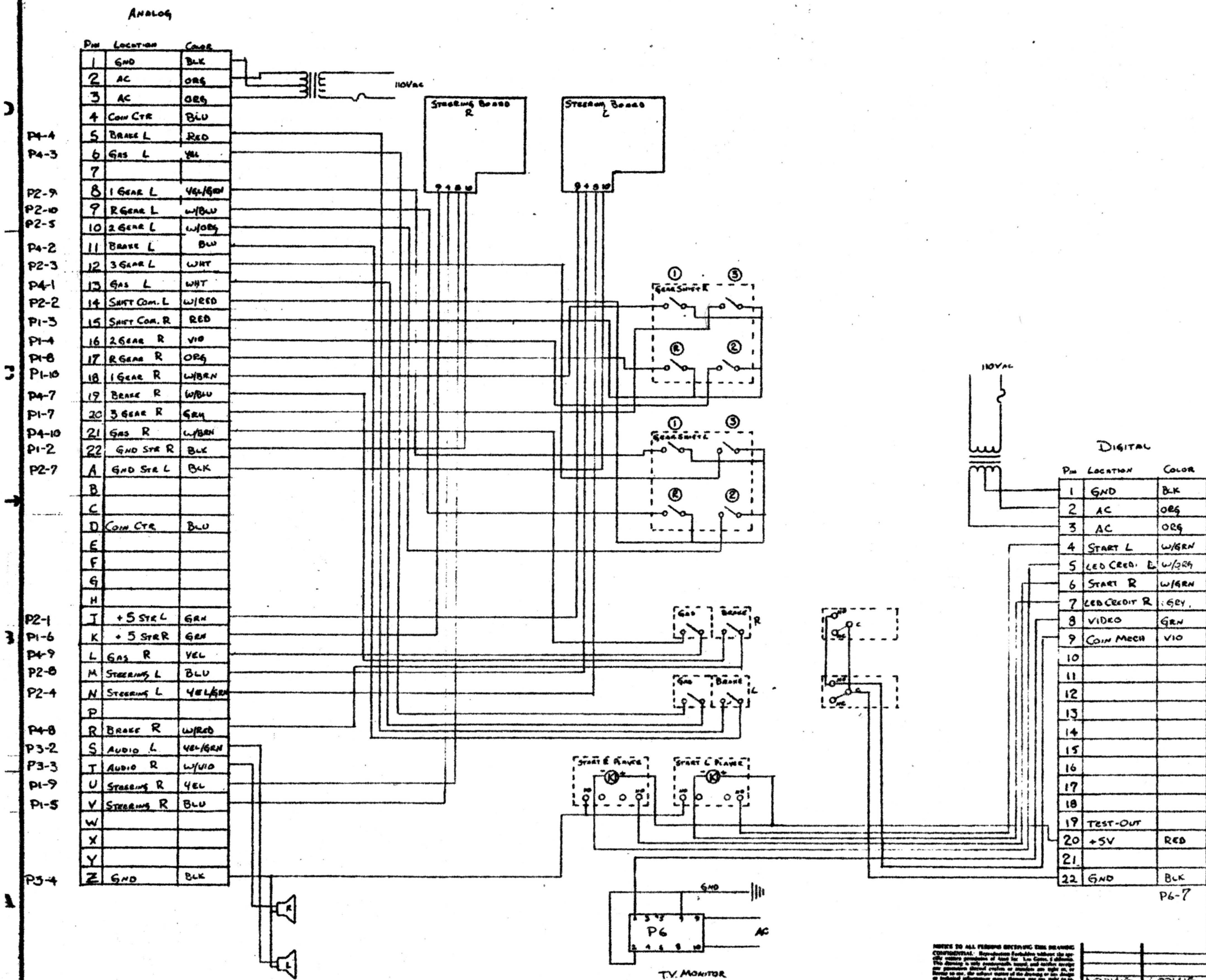
REV G

ASSY P

K4DKTA - STUFFING

A001793

1 of 1



SYM	DESCRIPTION	DATE
A	REL FOR PROD	7-30-79

INTERPRET THIS DRAWING PER USASI Y14.5

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON

MATERIAL

DRAWN BY C.L. Manning DATE 7/3/79

CHECKED

DESIGN ENGINEER

PROJECT ENGINEER

DOCUMENT CONTROL

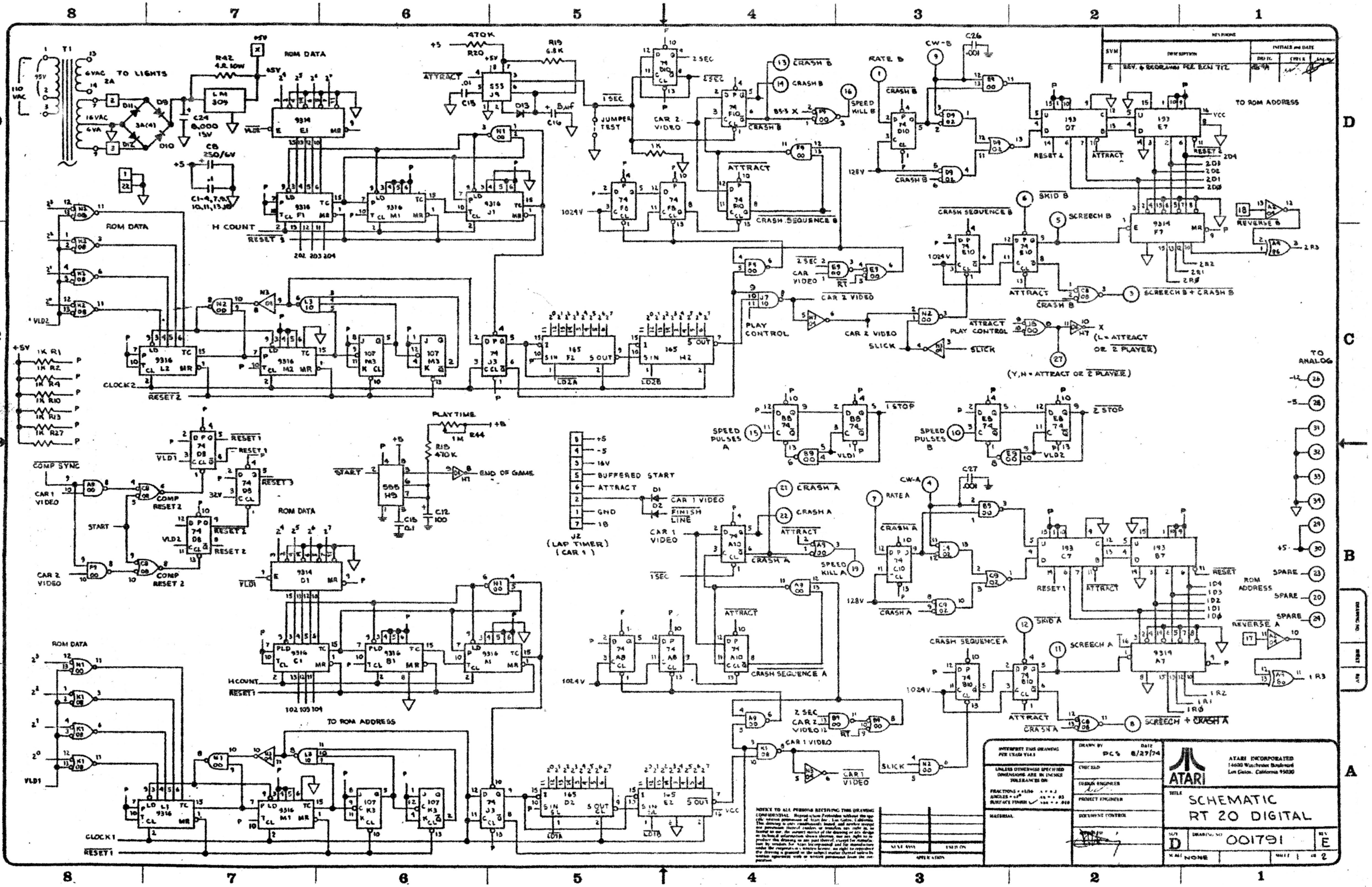
APPROVED

ATARI INCORPORATED
14600 Winchester Boulevard
Los Gatos, California 95030

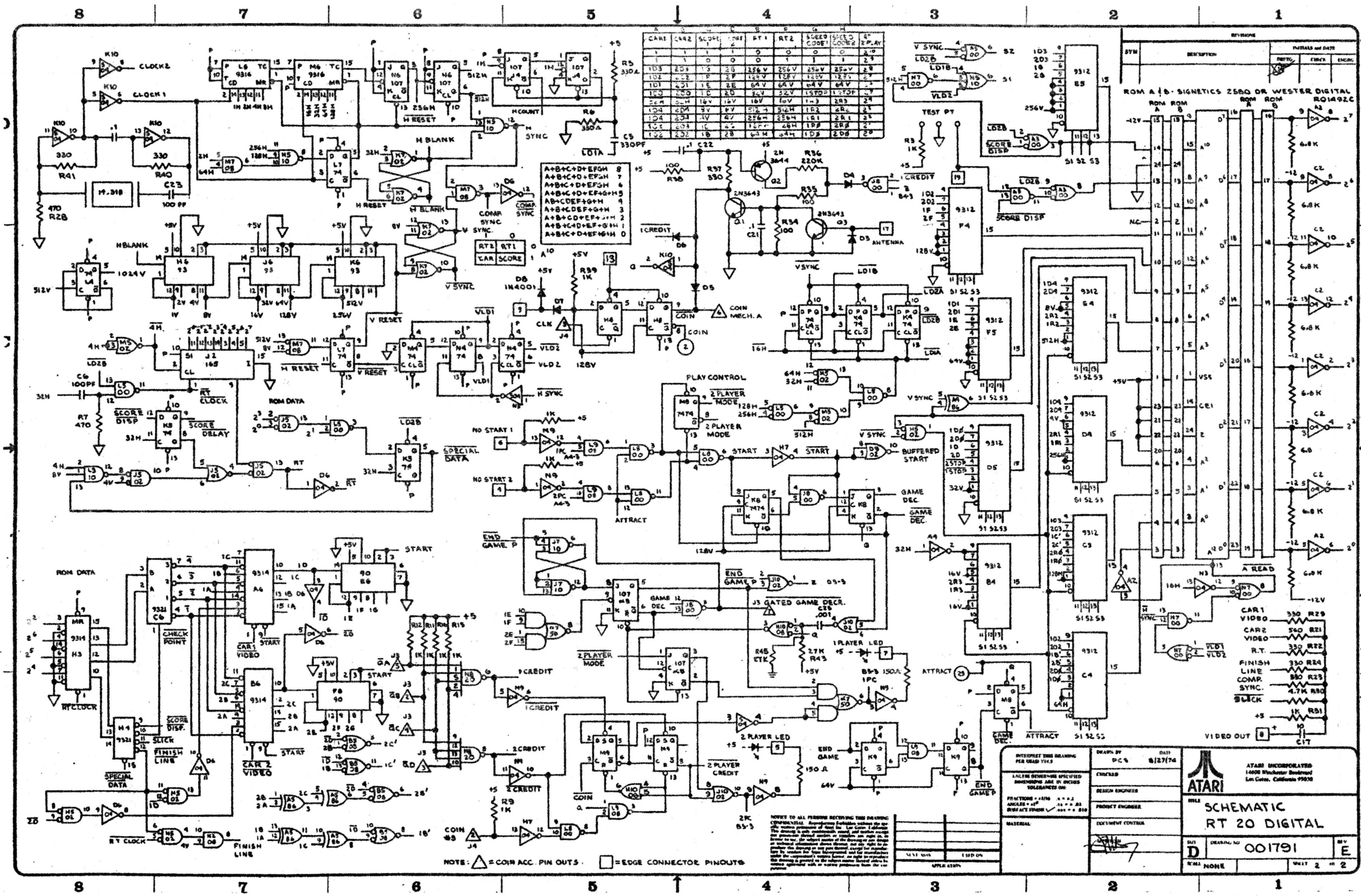
TITLE GRAN-TRAK 20
WIRING ENCLOSURE DIAGRAM

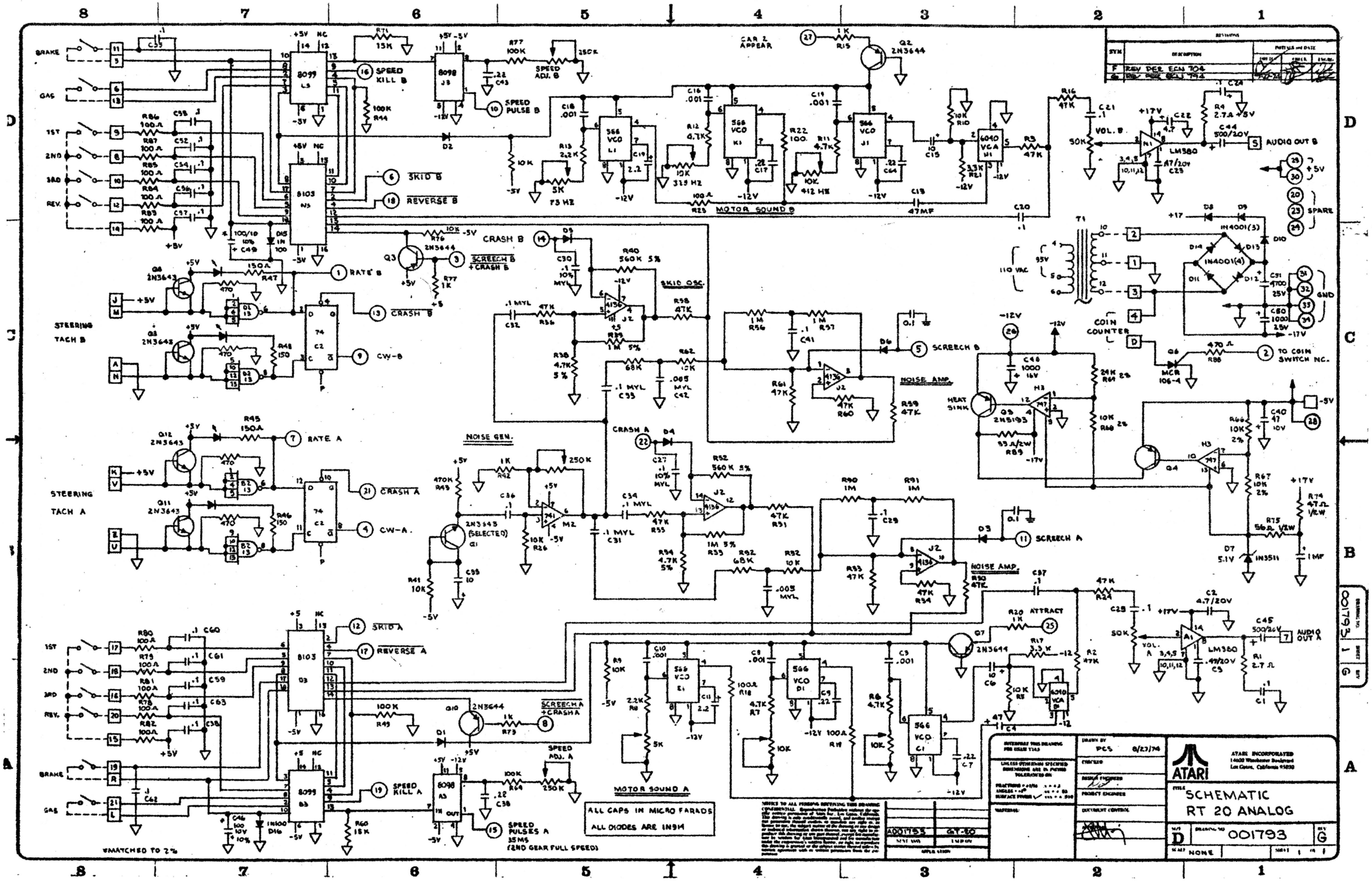
SIZE D DRAWING NO 001795 REV A

SCALE NONE SHEET 1 OF 1



SCHEMATIC
RT 20 DIGITAL
ATARI INCORPORATED
14600 Winchester Boulevard
Los Gatos, California 95030
001791
REV. & REDRAWN PER ECN 772
PCS 8/27/74
TO ANALOG
TO ROM ADDRESS
ROM DATA
LAP TIMER (CAR 1)


ROM A & B - SIGNETICS 2580 OR WESTER DIGITAL RO1492C
NOTE: △ = COIN ACC. PIN OUTS. □ = EDGE CONNECTOR PINOUTS
ATARI INCORPORATED
14600 Winchester Boulevard
Los Gatos, California 95030
SCHEMATIC
RT 20 DIGITAL
D
001791
E
NONE
SHEET 2 OF 2


ATARI
ATARI INCORPORATED
SCHEMATIC
RT 20 ANALOG
D
001793
G
NONE
PCS 8/27/74
F REV PER ECN 704
ALL CAPS IN MICRO FARADS
ALL DIODES ARE IN914
MOTOR SOUND A
MOTOR SOUND B
NOISE GEN.
NOISE AMP.
SKID OSC.
STEERING TACH A
STEERING TACH B
COIN COUNTER
TO COIN SWITCH NC.
AUDIO OUT A
AUDIO OUT B
110 VAC
HEAT SINK
CAR 2 APPEAR
SPEED KILL A
SPEED KILL B
SPEED PULSE B
SPEED PULSES A
35MS
(2ND GEAR FULL SPEED)
SPEED ADJ. A
SPEED ADJ. B
CRASH A
CRASH B
SCREECH A
SCREECH B
SKID A
SKID B
REVERSE A
REVERSE B
RATE A
RATE B
CW-A
CW-B
ATTRACT
SPARE
GND
BRAKE
GAS
1ST
2ND
3RD
REV.
*MATCHED TO 2%
A00755
GT-50

U.S.A.

CALIFORNIA

Advance Automatic Sales
1350 Howard St.
San Francisco, CA 94103
Tel: 415/431-1750

Circle International Co.
1433 W. Pico Blvd.
Los Angeles, CA 90015
Tel: 213/749-7405

C.A. Robinson
2301 W. Pico Blvd.
Los Angeles, CA 90006
Tel: 213/380-1160

COLORADO

Seeburg By Struve Dist. Co.
778 So. Santa Fe
Denver, CO 80223
Tel: 303/778-7778

FLORIDA

Eli Ross Dist. Inc.
807 Kipp St.
Jacksonville, FL 32207
Tel: 904/398-3371

Eli Ross Dist. Inc.
852 N.W. 71st St.
Miami, FL 33150
Tel: 305/836-1471

GEORGIA

Peach State Dist. Co.
1040 Boulevard Ave., S.E.
Atlanta, GA 30312
Tel: 912/743-1588

Peach State Dist. Co.
148 State St.
Macon, GA 31208
Tel: 912/743-1588

HAWAII

Atari Pacific
Suite 601
Pacific International Bldg.
677 Ala Moana Blvd.
Honolulu, HW 96813
Tel: 808/524-4083

ILLINOIS

Empire Dist. Co.
120 S. Sangamon St.
Chicago, IL 60607
Tel: 312/421-5200

INDIANA

Empire Dist. Co.
1333 Sadlier Circle (West Dr.)
Indianapolis, IN
Tel: 317/352-0466

IOWA

Phil Moss Co.
1420 Locust St.
Des Moines, IA 50309
Tel: 515/288-3331

LOUISIANA

Operator Sales
4122 Washington Ave.
New Orleans, LA 70125
Tel: 504/822-2370

S & H Dist. Co.
1500 Bolinger Rd.
Shreveport, LA 71103
Tel: 318/222-1642

MARYLAND

General Vending Sales
245 W. Biddle St.
Baltimore, MD 21201
Tel: 301/837-4119

MASSACHUSETTS

Robert Jones International
800 Providence Highway
Dedham, MA 02026
Tel: 617/329-4880

MICHIGAN

Empire Dist. of Mich., Inc.
19679 John R
Detroit, MI 48238
Tel: 313/368-8500

Empire Dist. Inc.
1939 S. Division
Grand Rapids, MI
Tel: 616/452-5663

MINNESOTA

Lieberman Music Co.
9549 Penn Ave., S.
Minneapolis, MN 55431
Tel: 612/888-5521

MISSOURI

L & R Dist.
1901 05 Demar Blvd.
St. Louis, MO 63103
Tel: 314/421-3622

Seeburg Central
1601 Forest
N. Kansas City, MO 64108
Tel: 816/421-4570

NEBRASKA

Central Dist. Co.
3814 Farnam St.
Omaha, NB 68131
Tel: 402/553-5300

NEVADA

Bally of Nevada
390 East 6th St.
Reno, NV 89502
Tel: 702/323-6157

NEW YORK

Davis Dist.
1056 Broadway
Albany, NY 12204
Tel: 518/434-4151

Davis Dist. Co.
1231 Main St.
Buffalo, NY 14209
Tel: 716/882-5500

Davis Distributing
56 N. Union St.
Rochester, NY 14607
Tel: 716/546-7848

Davis Dist. Co.
738 Erie Blvd. East
Syracuse, NY 13210
Tel: 315/471-6226

Musical Dist.
1161 Rogers Ave.
Brooklyn, NY 11226
Tel: 212/856-7720

NORTH CAROLINA

Brady Dist. Co.
1900 West Mooreland St.
Charlotte, NC 28208
Tel: 704/375-1713

OHIO

Cleveland Coin
2029 Prospect Ave.
Cleveland, OH 44115
Tel: 216/861-6715

Cleveland Coin
528 St. Clair St.
Toledo, OH 43602
Tel: 419/248-3359

Monroe Coin
2423 Payne Ave.
Cleveland, OH 44114
Tel: 216/781-4600

Seeburg of Ohio
457 Neilston St.
Columbus, OH 43215
Tel: 614/221-7821

OKLAHOMA

Culp Distributing
614 Sheridan Ave.
Oklahoma City, OK 93102
Tel: 405/232-9511

Sutherland Dist. Co.
705 N.W. 4th St.
Oklahoma City, OK 73102
Tel: 405/236-3691

OREGON

Dunis Dist. Co.
1140 S.E. 7th Ave.
Portland, OR 97214
Tel: 503/234-5491

PENNSYLVANIA

Active Amusement Machine Co.
66 N. Broad
Philadelphia, PA 19130
Tel: 215/684-1600

SOUTH CAROLINA

Peach State Dist.
1104 Shop St.
Columbia, SC 29202
Tel: 803/254-6928

TENNESSEE

Game Sales
444 Monroe
Memphis, TN 38104
Tel: 901/525-8351

Sammons Pennington
214 6th Ave., South
Nashville, TN 37203
Tel: 615/255-1129

TEXAS

All Coin
1811 S. Alamo St.
San Antonio, TX 78204
Tel: 512/222-2306

H. A. Franz
606 Dennis
Houston, TX 77006
Tel: 713/523-5574

O'Connor Dist. Co.
9030 Directors Row
Dallas, TX 75247
Tel: 214/631-0152

Sutherland Dist. Co.
2910 Tularosa Ave.
El Palo, TX 79903
Tel: 915/565-2725

UTAH

Struve Salt Lake City
276 W. First St.
Salt Lake City, UT 84101
Tel: 801/328-1636

WASHINGTON

Music Vend
100 Elliot Ave.
Seattle, WA 98119
Tel: 206/284-7740

WISCONSIN

Empire Dist. Inc.
2267 Main St.
Greenbay, WI 54301
Tel: 414/468-5200

EUROPE

BELGIUM

Ets C. Van Brabant
134 Belgielei
B-2000
Antwerp, Belgium
Tel: 391464
Cable: TONALTY Antwerp

ENGLAND

Atari U.K., Ltd.
7 Trent Lane
Castle Donington
Leicestershire, England
Tel: Derby 811224
Telex: 851377014
Cable: ATARI UK Breaston, Derbyshire

FRANCE

Socodimex
1 Quai de Grenelle
Paris, France 75015
Tel: 5770550
Telex: 84268461
Cable: SOCODIMEX Paris

FINLAND

Oy Gemco AB
Wallinsgatan 7
Helsfor 53, Finland
Tel: 71 18 33
Cable: GEMCO Helsinki

GERMANY (WEST)

Lowen Automaten
6530 Bingen/Rhine
Postfach 168
West Germany
Tel: 6721-15202
Telex: 841042222
Cable: LOWEN-AUTOMATEN
Bingen/Rhine

ITALY

Automatic Music
(Apparecchi Musicali Italiani)
Corso Filippo Turati, 28
Torino, Italy
Tel: 598-300/320
Telex: 84321226
Cable: AMI Torino

SPAIN

Sega S.A.
Juegos Recreativos
Apartado No. 16117
Sucursal No. 16
Madrid, Spain
Tel: 232-6640
Cable: SEGASTAR Madrid

Suministros Internaciales Gosteli
Travefera de Gracia 337
Barcelona 13, Spain
Cable: JUPITER Barcellona

SWITZERLAND

Amiro S.A.
25 Route des Acacias
Geneva 24, Switzerland
Tel: 022-42 22 10
Telex: 84522498
Cable: AMIRO S.A.

CANADA

CANADA

Dale Dist.
563 Minoru Blvd.
Richmond, British Columbia
Canada
Tel: 604/273-6691

Fountainhead Amusement Corp.
3150 Sartelon
St. Laurent, Quebec
Canada H4R1E3
Tel: 514/336-4305
Cable: FOUNTAINHEAD Montreal

FAR EAST/ASIA

AUSTRALIA

Hunter Electronics, Ltd.
48-52 Mountain Street
Broadway
Sydney N.S.W. 2007
Australia
Tel: 211-3188
Telex: 790 22442
Cable: Hunter Electronics,
c/o Commercial Bank of Australia

JAPAN

Atari Japan
1-19-11 Nakamura
Nerima-ku
Tokyo 176, Japan
Tel: 970-2171/6
Cable: ATARI JAPAN

NEW ZEALAND

Combined Enterprises, Ltd.
54 Upper Queen Lane
Auckland, New Zealand
Tel: 373-911
Cable: COMBINED
ENTERPRISES LTD.

CENTRAL & SOUTH AMERICA

BRASIL

Diverama
Rua Guaianazes, 209
Sao Paulo, Brasil
Tel: 32-8146, 35-8598
Cable: DIVERAMA Sao Paulo

Inelca S.A.
Industrias Electronicas
R. Vieira de Morais, 1890
Sao Paulo, Brasil
Cable: INELCARADIO Sao Paulo

PANAMA (REPUBLIC OF)

Cia Istomena de Diversiones S.A.
Apartado 6543
Panama 5, Republic of Panama
Tel: 62 3954
Cable: ISTAMCOR Panama

VENEZUELA

Intervenca
Apartado Chacao 61.125
Caracas 106, Venezuela
Tel: 33 97 21
Cable: INTERVENCA Caracas

1 - ROM 74181 HY BIRD
NO OIL SLICK

16 · K D-A CONV

2, ROM 74186 A - D
2 OIL SLICK

3 ROM 74187A & 8 8K
2 OIL SLICK

XP - 212
VP - 213
FREE PLAY